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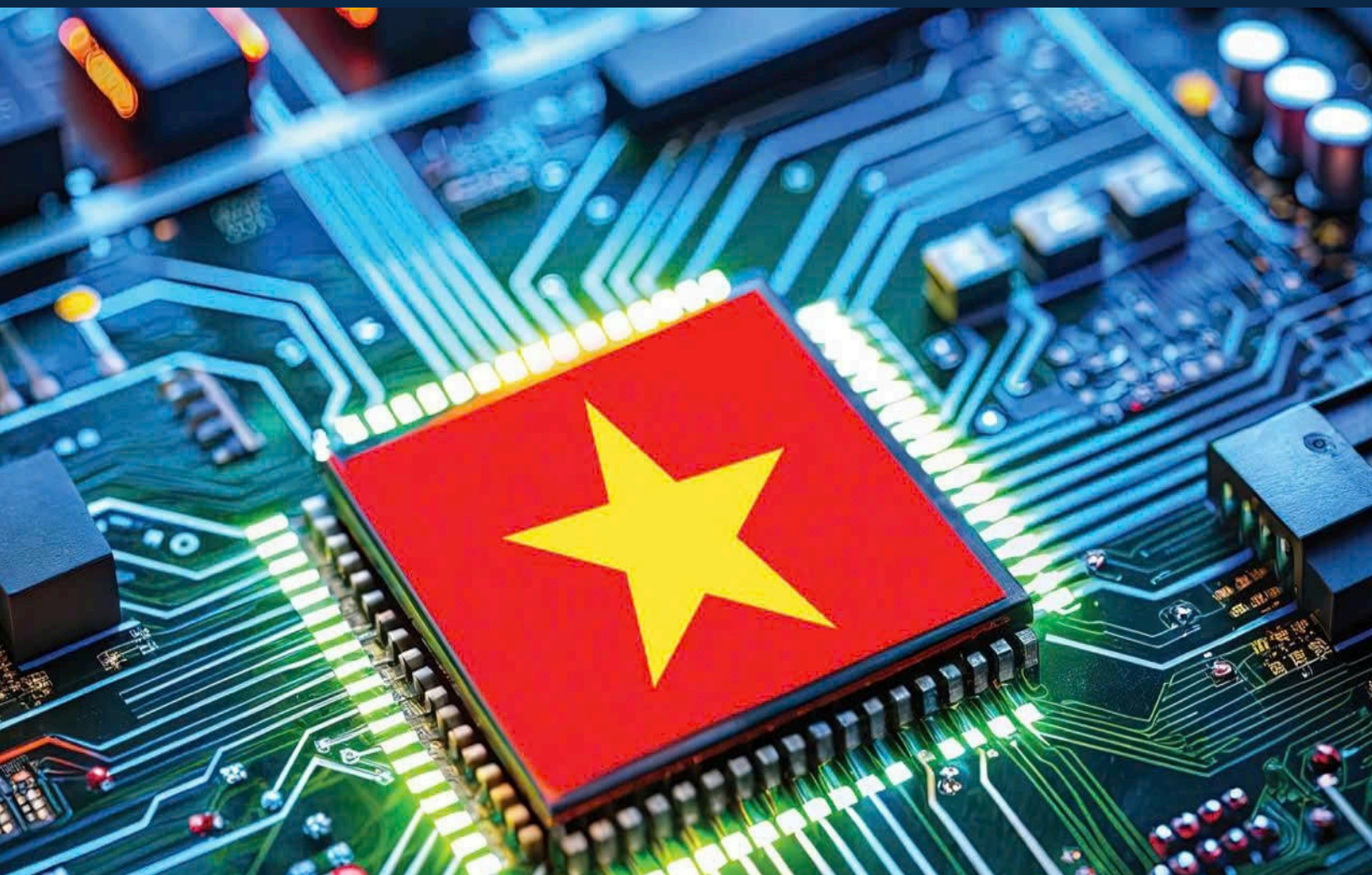
Enhancing Semiconductor Technology Protections in Vietnam

EDITED BY
AKHIL RAMESH AND ROB YORK



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Introduction

Over the course of 9 months, eight Vietnam Technology Policy fellows engaged in substantive research on policies related to Vietnam's semiconductor manufacturing ecosystem and developing a framework for successful U.S.-Vietnam cooperation in the semiconductor sector.

The eight fellows engaged in independent primary and secondary research alongside virtual meetings with industry experts and other guest speakers. In spring 2026, toward the end of their fellowship—sponsored by the Export Control and Related Border Security (EXBS) Program at the US Department of State— Pacific Forum organized a trip to Washington D.C., providing the fellows an opportunity to interact and learn from industry, government and academia—informing their research and analysis. Their fellowship concluded with policy papers offering actionable policy recommendations to enhance semiconductor technology protections and cooperation with the U.S. Find here, eight policy papers covering various areas of US-Vietnam semiconductor cooperation.

Akhil Ramesh
Chief Research and Development Officer
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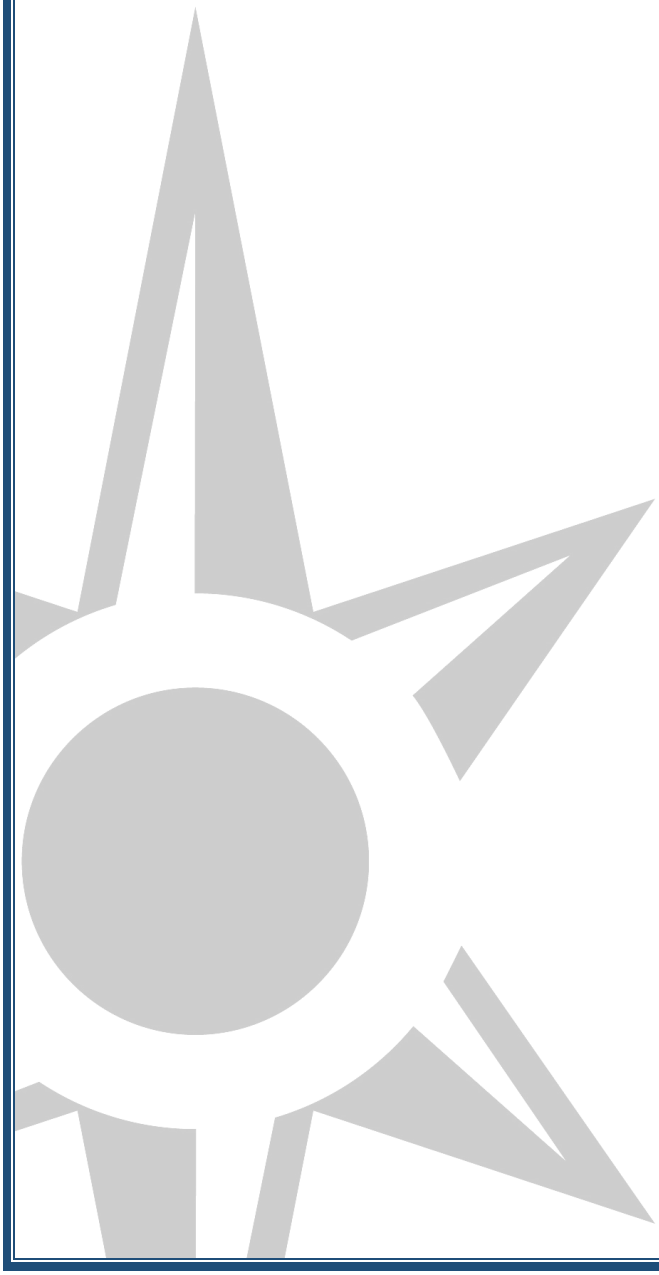
Legal Framework for Intellectual Property of Chip Designs in Vietnam's Collaborative AI and Semiconductor Industry

By
Huy Anh Nguyen



Executive Summary

Huy Anh Nguyen

Vietnam is emerging as a strategic player in the global semiconductor industry. The Vietnamese government has set forth an ambitious vision to establish a comprehensive domestic semiconductor ecosystem by 2050. As of 2025, Vietnamese enterprises contribute mainly to the supply chain in architecture design, RTL design, design verification, and assembly, test, and packaging. However, the country remains dependent on international partners for activities in various nodes of the value chain, such as semiconductor fabrication, where the protection and ownership of chip designs represent key challenges. This research examines the intellectual property framework governing collaborations between Vietnamese semiconductor design enterprises and foreign counterparts, with a focus on intangible technology transfer and ownership. The study identifies gaps and deficiencies in the Vietnamese legal system that may undermine effective IP protection, foster disputes, or create disincentives for cross-border collaboration and investment. Drawing on comparative analysis, it evaluates best practices from leading semiconductor-producing jurisdictions, with emphasis on Southeast Asian competitors, and situates Vietnam's legal approach within its broader commitments under international treaties and policies. The study proposes targeted legal reforms and policy recommendations to strengthen Vietnam's IP safeguards, enhance legal clarity, and foster a more competitive and secure environment for semiconductor innovation.

Introduction

In a legal framework, intellectual property rights (IPR) refers to ideas, inventions, and creative works that gain property-like status through public recognition. These rights provide creators or inventors with exclusive privileges to monetize their innovations or reputation. Various protections exist, including patents, copyrights, and trademarks.[1] [2] IPR plays an essential role in identifying, strategizing, commercializing, implementing, and safeguarding inventions and creative outputs. Industries tailor their IPR policies, management approaches, and strategies to suit their specific sectors.[3]

In the semiconductor industry, integrated circuit (IC) layout designs represent human intellectual creations, qualifying them as intellectual property (IP). IC layout designs are fundamental to semiconductor chips, defining the precise physical arrangement of transistors, interconnects, and components that ensure functionality, performance, and manufacturability. Their importance has grown with AI, as optimized layouts enable efficient, high-density chips tailored for AI workloads.[4]

While the creation and updating of a IC layout design is usually the result of an enormous investment, both in financial terms and in terms of the time required from highly qualified experts, the copying of such a layout design may cost only a fraction of the original investment. Chip pirates can duplicate these designs cheaply and quickly, by stripping away the protective plastic or ceramic casing and photographing the transparent silicon layers.[5] To prevent unauthorized copying of layout designs and to provide incentives for investing in this field, under WIPO, the layout design (topography) of IC is protected under a sui generis IP system.[6]

However, in the dynamic world of technology, sharing chip design rights has become a trend. Companies may choose to team up or license their designs to others, fostering innovation and the birth of new products without reinventing the wheel.[7] In essence, the current landscape of chip design ownership and sharing is a delicate mixture between safeguarding IP and encouraging collaboration to drive progress and push the boundaries of technology.

Developing System-on-Chips (SoCs) by integrating reusable IP core modules with a blend of hardware/software design and advanced sub-micron/nanometer processes now drives chip innovation. Leveraging pre-built IP cores, standardized IC modules, and files accelerates design timelines and boosts reliability. In fact, over 90% of today's industry SoCs rely on IP cores, many of which are recycled across multiple projects.

The IP core sector, a cornerstone of the chip market, remains concentrated among a handful of leaders. The top 10 providers command 82.6% market share, expanding at 12.5% annually—outpacing the broader industry's 9% average. Of the top 50 suppliers, 30 hail from the US, though Chinese firms are gaining ground. Global IP core sales hit $5.2 billion in 2021, with forecasts reaching $7 billion by 2026 and $9 billion by 2030 at a steady 5–6% compound annual growth rate.[8]

Vietnam is the long-term provider in IC layouts design for tech giants.[9] And the biggest chip companies in the world such as Qualcomm, SAP,

[1] Drahos, Peter. "The universality of intellectual property rights: origins and development." *Intellectual Property and Human Rights. Geneva: World Intellectual Property Organization* (1999): 18.

[2] Spinello, Richard A. "Intellectual property rights." *Library hi tech* 25.1 (2007): 15.

[3] Priyana, Yana. "Intellectual Property Rights Relating to Integrated Circuit Layout Design: India, Bangladesh, and United States Perspectives." *The Easta Journal Law and Human Rights* 1.01 (2022): 03-05.

[4] Maida, Payal, Yogesh Patidar, and M. P. Ujjain. "Integration of Artificial Intelligence in Electronic Circuit Design for Enhanced Performance." *International Journal of Engineering Applied Science and ManagementISSN (Online)* (2024).

[5] Priyana, Yana (n 3)

[6] World Intellectual Property Organization. "Layout Designs (Topographies) of Integrated Circuits." *WIPO*, https://www.wipo.int/en/web/patents/topics/integrated_circuits.

[7] Chu, Po-Young, and Wan-Chen Chen. "Open business models: A case study of System-on-a-Chip (SoC) design foundry in the integrated circuit (IC) industry." *African Journal of Business Management* 5.21 (2011): 8536.

[8] "Silicon Integrated Circuit Intellectual Properties Design." *Embedded*, 30 Oct. 2024, https://www.embedded.com/silicon-integrated-circuit-intellectual-properties-design/.

[9] Binh Minh. "Vietnamese engineers sell IP cores that make chips to tech giants." *VietnamNet*, n.d., https://vietnamnet.vn/en/vietnamese-engineers-sell-ip-cores-that-make-chips-to-tech-giants-2283539.html.

Infineon have opened R&D labs in Vietnam.[10] But the collaboration between local companies and international corporations is still limited. Foreign investors in semiconductors emphasize registering IP assets before any transfer, indicating reluctance to share without robust legal safeguards in place.[11] The IP law in Vietnam does not yet have specific articles on IC layout designs, as seen in some other countries. While developing such safeguards is crucial in the race for semiconductor industry development, Vietnam's IP law does not yet have specific articles on IC layout designs, as seen in some other countries.

Especially, on April 30, 2026, the US Office of the Trade Representative (USTR) issued its annual Special 301 Report, which evaluates how foreign intellectual property laws such as copyright, patents and trademarks, and enforcement affect US companies and products.[12] And it designated Vietnam as a Priority Foreign Country (PFC). This is the highest category in the Special 301 system, above the Watch List and Priority Watch List, and it is reserved for trading partners USTR views as having the most serious IP-related problems. Vietnam was the only country to receive that label in 2026, and the first to do so since 2013. The report also points to enforcement disruption caused by Vietnam's 2025 administrative restructuring and says USTR continued to rely on administrative remedies that, in its view, do not create enough deterrence. Moreover, on May 29, 2026, US Trade Representative Jamieson Greer initiated an investigation of Vietnam under Section 301 of the Trade Act of 1974. The investigation will seek to determine whether Vietnam's persistent failure to resolve long-standing concerns about IP protection and enforcement is unreasonable or discriminatory and burdens or restricts US commerce.[13] Although the five grounds do not include IP registration and cooperation, the report highlights widespread violations of IP laws and weak enforcement across industries, and it underscores the need for stronger regulation in the field of IC layout design.

Research Layout

What is the legal framework for Intellectual Property of Chip Designs in Vietnam's Collaborative AI and Semiconductor Industry? First, this research will look up to the core and the flexible part of the international instrument on protection of IC Layout Designs. Then the current legal framework in IC layout design in Vietnam is presented. Then, this research will look up the IP policy in chip design in multiple countries to find the main elements of the Integrated Circuit Layout Design Act. This research will focus on the IC layout design act in pioneer developed countries such as the US, EU, Japan, etc. then those that have concentrated in the semiconductor industry such as India, China, Singapore, New Zealand and so on. This research will focus more on the Semiconductor Chip Protection Act in the US It protects topographies of semiconductor chips under a dedicated statute, a model often cited in comparative discussions of layout-design protection frameworks alongside the IPIC/TRIPS architecture based on history. The effectiveness of the IC layout design act in these countries in the IP and innovation aspect is presented. Then, the recent advancement of the IC design layout act in China is mentioned.

Based on the suitability assessment, recommendations are formulated for Vietnam on how to either integrate suitable aspects, learn from the experiences to build their own policies. As semiconductor is the race between some Southeast Asian countries, which aspect of the act on this needs to be focused on or to be considered the competitive edge of Vietnam is also mentioned. Later, it evaluates the suitability and feasibility of adapting or incorporating elements from these policies into the frameworks of Vietnam, considering their unique economic and legal contexts. The overall amendment also needs to be harmonized with international treaties and regulations. The concern for future development of AI in IC layout design is also explored. Finally, the limitation of this research will be mentioned.

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[10] Cong Tung, Nguyen. "Tug of war: Vietnam's strategic pragmatism in the US-China tech race." *Political Science* 77.2-3 (2025): 297.

[11] Yinug, Falan. "Challenges to foreign investment in high-tech semiconductor production in China." *J. Int'l Com. & Econ.* 2 (2009): 97.

[12] Office of the United States Trade Representative. 2026 Special 301 Report. 30 Apr. 2026. https://ustr.gov/sites/default/files/files/Press/Releases/2026/2026%20Special%20301%20Report.pdf

[13] Office of the United States Trade Representative. "USTR Announces Section 301 Investigation Into Vietnam's Acts, Policies, and Practices Related to Intellectual Property." Press release, 28 May 2026. https://ustr.gov/about/policy-offices/press-office/press-releases/2026/may/ustr-announces-section-301-investigation-vietnams-acts-policies-and-practices-related-intellectual.

Methodology

For this research, I use the comparative legal methodology. Technology has made our world a global village but the legal framework of each country and territory is still different. The purpose and approach of comparative law aim to establish a solid methodological framework for deeper comprehension of legal systems across countries.[14] This framework helps foster insight and knowledge, potentially encouraging some harmonization on key matters or, at the very least, achieving a shared understanding.[15] A large number of IP scholars has turned to comparative legal analysis to address research questions related to IP law, both to assess the current national and international laws as well as propose amendments to these laws.[16] Comparative analysis includes the revision of existing laws, or the implementation of new standards deriving from international or other free trade agreements, or from national initiative.[17] Especially in the case of the cross-functional field of the semiconductor industry, when scholars mostly agree that the relevance of comparative legal methods goes beyond the understanding of legal systems and extends to international relations, economics, political science, and diplomatic studies.[18]

A. The International Instrument on Protection of IC Layout Designs

The Core Elements

The United States pioneered protection for semiconductor chip layouts with the Semiconductor Chip Protection Act (SCPA) of 1984 through sui generis rights for mask works, separate from patents or copyrights, influencing protections globally. Japan followed in 1985 with the Act on the Circuit Layout of a Semiconductor Integrated Circuits (JCLRA). An EU directive (87/54/EEC) mandated member states to enact laws safeguarding semiconductor product topographies, defining "topography," originality, scope limits, and formalities (including the "T" marking option), and conferring exclusive rights for protected topographies via national laws.

A 1989 diplomatic conference in Washington DC, produced the Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty or Washington Treaty), open to WIPO/UN members and qualifying organizations. The WTO TRIPS Agreement incorporates the IPIC Treaty with changes. From a US view, TRIPS exported SCPA-like standards worldwide, harmonizing IP while enforcing reciprocity through trade rules.[19]

The TRIPS Agreement protects layout-designs (topographies) of semiconductor chips IC in Section 6 (Articles 35-38). Article 35 of TRIPS links to the IPIC Treaty by "Members agree to protect the layout design (topography) of the IC layout design (in this Agreement referred to as "layout design") under Articles 2 to 7 (other than paragraph 3 of Article 6), Article 12, and paragraph 3 of Article 16 of the Agreement concerning IP in connection with the IC and, in addition, to comply with the following provisions."

Article 2 of the IPIC Treaty provides the following definitions of IC and layout designs: An IC is a product, in a final or intermediate form, in which the elements, at least one of which is an active element, and some or all of the interconnections are integrally formed in and/or on a piece of material and which are intended to perform a function electronically.[20] "Layout design (topography)" means the three-dimensional disposition, however, stated, of the elements, at least one of which is an active element, and some or all of the IC interconnects, or similar three-dimensional elements. dimensional disposition prepared for the integrated circuit intended for manufacture.[21]

In article 36, the rights holder's exclusive rights also cover items incorporating an IC in which a protected

[14] Eberle, Edward J. "The methodology of comparative law." *Roger Williams University Law Review* 16.1 (2011): 2.

[15] ibid.

[16] Dutfield, Graham, and Uma Suthersanen. "Harmonisation or differentiation in intellectual property protection? The lessons of history." *Prometheus* 23.2 (2005): 137.

[17] Kur, Annette, and Martin RF Senftleben. *European trade mark law–a commentary*. Oxford University Press, 2017.

[18] Legrand, Pierre. "On the singularity of law." *Harvard International Law Journal* 47.2 (2006): 517.

[19] Radomsky, Leon. "Sixteen Years After the Passage of the US Semiconductor Chip Protection Act: Is International Protection Working?." *Berkeley Technology Law Journal* (2000): 1053.

[20] Gervais, Daniel. "TRIPS Agreement." *Encyclopedia of Law and Economics*. Cham: Springer Nature Switzerland, 2026. 2441.

[21] ibid.

layout design is incorporated, to the extent that it continues to contain an unauthorized reproduced layout design. Article 37 allows exceptions for innocent performers unaware of unlawful reproduction or for research purposes. These exceptions prevent blocking independent innovation or compatibility improvements. Circumstances under which layout designs can be used without the consent of the rights holder are more restricted. Article 38 sets the term of protection at least 10 years from the date of submission of the application or the world's first commercial exploitation. But Members can provide a period of protection of 15 years from the creation of the layout design. TRIPS Article 31(c) restricts compulsory licensing of semiconductor technology to public non-commercial use or anti-competitive remedies. Trade secrets in semiconductor production also gain explicit multilateral protection under Article 39.

The Flexible Part

Article 35 of the TRIPS Agreement incorporates provisions from the IPIC Treaty limiting layout-design protection for IC to acts within the protecting country, such as reproduction or distribution there, while granting WTO nationals national treatment (Article 3) and most-favored-nation treatment (Article 4) across members, with remedies and enforcement remaining jurisdiction-specific. Protection does not extend abroad, a layout-design registered in one country requires separate filings elsewhere, and disputes proceed via WTO mechanisms, but enforcement depends on each state's courts or agencies, fostering reciprocal cross-border trade without eroding sovereignty. Complementing this, TRIPS Article 6 permits members to establish national, regional, or international exhaustion regimes for all IP, including ICs under Articles 35-38, free from WTO dispute settlement challenges (subject to Articles 3 and 4), where exhaustion limits IP owners' control over goods post-first authorized sale to promote free trade. This framework balances IP incentives with exceptions like reverse engineering (IPIC Article 6(2)) and exhaustion flexibility (Article 6(5)).

B. IC Layout Designs under Vietnam's IP Law

Vietnam's emergence as a premier global technology hub hinges on its IP laws, which confront substantial hurdles in the digital era.[22] Vietnam's IP laws depend heavily on an effective supporting international legal and institutional structure. The country participates in key global and regional copyright agreements, such as the Berne Convention, the bilateral US-Vietnam Agreement on the Settlement of Copyright Interactions, US-Vietnam trade deals, and the Switzerland Agreement on the Protection of IP Rights.[23]

Vietnam has continuously improved its IP protection system over the past 16 years. Vietnam IP Law (Law No. 42/2019/QH14) has undergone substantial changes in 2009, 2019, and 2021,[24] especially the revision on June 14, 2019 to meet the Comprehensive and Progressive Agreement for Trans-Pacific Partnership (CPTPP) requirements after the agreement entered into force on January 14, 2019. As Vietnam continues to open to the rest of the world, protecting IP is essential for the country's economy and society as a whole.[25]

Thus, global technological advancement will necessitate the establishment of additional transnational regulatory systems. Depending on the strength or weakness of the current IP law regime, changes to IP law might alter incentives in ways that favor specific fields, industries, or closely monitored areas of development. It requires modifications to the Vietnam IP laws. The proposed legislation should incorporate Vietnam's commitments under existing international treaties (EVFTA, CPTPP, The Hague Agreement, WCT Agreement, WPPT Agreement, and Budapest Treaty).[26]

Vietnam adheres to the TRIPS Agreement as a member state. Therefore, Vietnam's IP law aligns

[22] Sidorenko, Elina L., and Pierre Von Arx. "Transformation of law in the context of digitalization: Defining the correct priorities." *Digital law journal* 1.1 (2020): 28.

[23] Nguyen, Dao Ngoc Anh, V. P. Nguyen, and Kim Hieu Bui. "Vietnam's regulation on intellectual property rights protection: The context of digital transformation." *International Journal for the Semiotics of Law-Revue internationale de Sémiotique juridique* 37.1 (2024): 263.

[24] Nguyen Phan, Khoi. "Protecting Intellectual Property Rights in Vietnam: Opportunities and Challenges." *Challenges of Governance: Development and Regional Integration in Southeast Asia and ASEAN* (2021): 122.

[25] Nguyen, Dao Ngoc Anh, V. P. Nguyen, and Kim Hieu Bui. (n 23)

[26] Gioi, Phan Minh. "Impact Of International Trade Agreements On Commercial Law In Vietnam." *Russian Law Journal* 11.3 (2023): 2799.

with TRIPS requirements. According to Vietnamese law, an IC layout-design refers to the three-dimensional arrangement of circuit components and their interconnections within an IC. The legal framework for IC layout designs falls under the umbrella of broader IP law. Industrial property rights for these designs are secured either through a formal protection title granted by the Vietnam National Office of Intellectual Property, following standard domestic registration protocols or through the recognition of international registrations as governed by treaties to which Vietnam is a party.

In Vietnam, layout-designs qualify for protection if they demonstrate originality and commercial novelty. A design is original when it stems from the creator's own intellectual effort and was not commonplace among layout-design creators or IC manufacturers at creation time. In terms of commercial novelty, a layout-design is considered novel only if it has not been commercially exploited anywhere in the world prior to its filing date. Commercial exploitation is defined as the public distribution for profit of either the semiconductor IC created from those layout-designs or any finished products that incorporate such circuits. Protection via registration certificate begins at issuance and ends at the earliest of ten years from filing date, 10 years from first commercial exploitation worldwide by the rights holder or licensee, or fifteen years from creation date.[27]

C. Comparative Analysis of IC Layout Design Acts Across Countries

The Definition of IC Layout-Designs Under Existing IPR

Protecting IC layout-designs under existing IPR faces challenges. The unique characteristics of IC layout-designs hinder their alignment with other IPR types. Functionally specific, they do not match copyright's expressive nature. Although layout-design protection demands novelty akin to inventions, invention novelty is rigorously absolute, whereas layout-design novelty is merely "commercial novelty," far less demanding. Moreover, layout-designs fail to satisfy the inventive step required for patents. For industrial designs, IC layouts do not qualify, as they involve internal physical placements of electronic-function elements rather than a product's external appearance. These factors led the TRIPS Agreement to grant member countries flexibility in protecting layout-designs, tailored to national approaches. It explicitly allows states to employ copyright, patents, utility models, industrial designs, unfair competition laws, or any other mechanism for layout-designs. Countries may thus safeguard them via existing IPR frameworks or enact distinct legislation. Trade secrets represent another IPR option that applicants often consider for layout-designs. Yet, since layout-designs are readily reverse-engineered and replicated, trade secrets offer limited effectiveness here. While most countries follow the TRIPS agreement to make clear legal definitions for development of this field, countries with focus in the semiconductor industry all over the world have implemented specific regulatory frameworks for IC layout designs. Canada has the Integrated Circuit Topography Act (1990). South Korea has The Act on the Layout-Designs of Semiconductor Integrated Circuits (1992). Moreover, in India, the Layout Designs of Semiconductor Integrated Circuits Act, 2000 recognizes a new IP category called 'layout designs' for semiconductor IC, as outlined in section 2(h) of the Act.[28] [29] In Japan, in 1985, The Act on the Circuit Layout of a Semiconductor Integrated Circuits established "layout design licenses" separating from patents, copyrights, or trademarks.

Specific Reverse-Engineering Rules

Reverse engineering poses a significant concern for both IPR holders and IC designers. It serves as a standard method to analyze a device's functionality, power usage, and performance.[30] However, it also endangers proprietary design information.[31] The SCPA explicitly permits reverse engineering to

[27] Intellectual Property Office of Vietnam. "Other Requests." *IP Viet Nam*, https://www.ipvietnam.gov.vn/web/english/other-request. Accessed 25 May 2026.

[28] Varma, Pothuru Sashank. "Protection of Layout Design for Integrated Circuits Comparative Study between India and USA." *Issue 5 Int'l JL Mgmt. & Human.* 4 (2021): 24.

[29] Bindal, Saurabh. "The Semiconductor Integrated Circuit Layout Design Act 2000 in India and the mischief of freedom of infringement." *Journal of Intellectual Property Law & Practice* 10.5 (2015): 380.

[30] McLoughlin, Ian. "Reverse engineering of embedded consumer electronic systems." *2011 IEEE 15th International Symposium on Consumer Electronics (ISCE)*. IEEE, 2011.

[31] Colombier, Brice, and Lilian Bossuet. "Survey of hardware protection of design data for integrated circuits

photograph, study, and analyze a protected mask work for understanding its circuitry, logic flow, and organization, allowing incorporation of such analysis into an *original* mask work. This serves as a defense to infringement, where courts raise the bar from "substantial similarity" to requiring proof of "substantially identical" copying (slavish copying) when supported by evidence like a paper trail of independent design efforts—a recognized two-prong test involving substantial differences and documented toil.[32] The law encourages innovation through this analytical exception but mandates originality in the resulting work, without authorizing direct integration into copies of the original mask work itself.[33]

China's Regulations on the Protection of Layout-Designs of Integrated Circuits allow reverse engineering by photographing and analyzing chips to understand circuit principles, like SCPA allowances. Courts enforce this by prohibiting "direct copying" of layouts, even original parts for commercial products, treating reproduction as infringement regardless of size. These contrast with EU's, Japan's and South Korea's laws, which align closely with IPIC Treaty standards.

The HiTrend (HiPower) v. Renergy case is a notable Chinese IP dispute involving infringement of an IC layout design right. This focuses on unauthorized replication, aligning with anti-slavish copying enforcement. HiTrend Technology (Shanghai) accused Renergy Micro-Technologies (Shenzhen) of copying specific layouts from HiTrend's registered IC design ATT7021AU, including the "layout for connection of digital ground rack and analogue ground rack" and "independent booster circuit layout." Renergy admitted accessing the design through former HiTrend employees but did not reverse-engineer it, instead directly incorporating parts into its RN8209 and RN8209G chips for manufacturing and sale. The Shanghai No. 1 Intermediate People's Court ruled on December 24, 2013, that Renergy must cease infringement and compensate HiTrend RMB 3.2 million (about $500,000 at the time) for economic losses and reasonable expenses; other claims by HiTrend, including a public apology and higher damages (RMB 15 million), were rejected.[34] The courts found Renergy's actions violated HiTrend's exclusive rights under China's Regulations on the Protection of Layout Designs of Integrated Circuits (Article 23 did not apply due to admitted copying, not independent creation). Compensation was based on Renergy's unverified sales claims (10 million units advertised online), but limited since the copied elements were minor (small area, not core functions) and no profit evidence was proven for full chip similarity. This emphasized savings in R&D time and market advantage gained by Renergy as factors in damages. This judgment provides a precise interpretation of how the law applies in this case while setting clear standards for identifying layout design infringement. It helps designers distinguish between permissible references and outright plagiarism. The ruling holds vital practical value for protecting layout designs and fostering IC industry development.

Automatic Registration or Manual Signup

Differences from Vietnam, Singapore, Hong Kong, New Zealand and Australia do not require layout-designs to be registered and protected on the basis of the issued certificate but will be automatically protected from the time they are presented in commercial exploitation. Singapore provides automatic protection for original layout-designs of IC without requiring registration or deposit with IPOS, effective for qualifying owners like citizens or WTO members upon creation. Hong Kong's Layout-Design (Topography) of Integrated Circuits Ordinance (Cap. 445, enacted 1994, amended through 2025) protects original topographies automatically upon creation, without mandatory registration. In Australia, protection for IC layout design is unregistered and automatic under the Circuit Layouts Act 1989. Rights simply expire after the statutory term, or owners may choose not to enforce them. New Zealand similarly grants unregistered, automatic protection under the Layout Designs Act 1994 for original designs first

and intellectual properties." *IET Computers & Digital Techniques* 8.6 (2014): 278.

[32] Kasch, Steven P. "The semiconductor chip protection act: past, present, and future." *High Technology Law Journal* 7.1 (1992): 80.

[33] Evans, Tonya M. "Reverse Engineering IP." Marquette Intellectual Property Law Review, vol. 17, 2013, pp.96.. Marquette University Law School Scholarship Repository.

[34] HiTrend Technology (Shanghai) Co., Ltd. v. Renergy Micro-Technologies (Shenzhen) Co., Ltd. & Shanghai Yachuang Texin Electronics Co., Ltd., (2014) HGMS (Z) ZZ No. 12 (Shanghai High People's Court). https://www.wipo.int/wipolex/en/text/578398

commercially exploited or made in eligible countries, without a formal registration system. Automatic systems simplify access by eliminating bureaucratic hurdles and costs, enabling quick rights establishment for creators worldwide. They promote innovation in fast-paced fields like semiconductors by avoiding delays. But compared to registered rights, it can be harder to prove ownership or originality in legal disputes because ownership during disputes relies on internal records, which can weaken enforcement and lead to costly litigation without public notice of the right. Registration provides a public record, prima facie evidence of validity, and easier enforcement against infringers, with examination ensuring quality. It deters copying through official certificates and opposition mechanisms. Drawbacks include fees, processing delays, potentially months, and risks of refusal if not novel.

Different Explanation of Term

Vietnam's IP Law takes effect from issuance and expires at the earliest of, end of 10 years from filing date, 10 years from first commercial exploitation worldwide by the rights holder or authorized party, or 15 years from creation, differing from the simpler 10-year terms in the US, EU, and Japan.

The US SCPA, 17 USC. Chapter 9 provides a single 10-year term for mask works, starting from registration or first commercial exploitation worldwide, whichever first. EU Directive 87/54/EE offers 10 years from first commercial exploitation or filing, whichever earlier, across member states. Japan's Act on the Circuit Layout of a Semiconductor Integrated Circuits grants a 10-year license term from registration date, non-renewable.

In China, “The protection period of the exclusive right to layout-design is 10 years, calculated from the date of application for registration of the layout-design or the date of first commercial exploitation anywhere in the world, whichever is earlier. However, regardless of whether it is registered or commercially exploited, a layout-design shall no longer be protected by these Regulations 15 years after its creation.”

Reciprocal Protection

Based on the TRIPS Agreement, multiple countries provide protection for foreigners of countries with equivalent policy. This part is completely missing in the IC layout design policy of Vietnam. US SCPA Section 902 provides reciprocity for foreign mask works if the foreign country offers equivalent protection via treaty or presidential proclamation. Integrated Circuit Topography Act of Canada reciprocal protection applies to nationals from listed countries that provide substantially equal protection to Canadians, as certified in official schedules. EU Directive 87/54/EEC permits third-country agreements. This framework promotes global harmonization for IC layout protection. In New Zealand, Protection arises automatically for layout designs first exploited or created by residents of "eligible countries," defined by mutual international agreements or reciprocal arrangements.

In Asia, Taiwan's Integrated Circuit Layout Protection Act (Article 5) grants foreign owners registration rights if their home country offers reciprocal protection via treaties, verified equivalence, or approved agreements with ROC organizations. The Act on the Layout-Designs of Semiconductor Integrated Circuits in South Korea protects foreign layout-designs through treaties South Korea has acceded to or signed. Hong Kong's 2024 Amendment Regulation designates qualifying countries for reciprocal IC layout-design protection.

National Security Clause in Southeast Asia

Specially in some Southeast Asia countries, national security and defense needs are mentioned in the IC layout design acts. Singapore's Layout-Designs of Integrated Circuits Act (Chapter 159A) includes a targeted government-use exception under Sections 23-25 for national defense or civil defense emergencies. This allows the government or authorized persons to use protected IC layout-designs without infringing the owner's rights, provided it's for public non-commercial purposes. The government must notify the qualified owner as soon as practicable after the act, especially in urgent situations.[35] In Thailand, section 34 of the Protection of Layout—Designs of Integrated Circuits Act, B.E. 2543 (2000) permits state agencies, enterprises, or authorities to apply for authorization to use layout-design rights for national defense, security, safety,

[35] Layout-Designs of Integrated Circuits Act (Chapter 159A) (Revised Edition 2000, amended up to the Supreme Court of Judicature (Amendment) Act 2019), Singapore, 16.

health, environment, or other public non-commercial interests. Section 35 grants the Prime Minister, with Cabinet approval, power during war or emergencies to order such use, with equitable remuneration and prompt notification to rights holders.[36] In Malaysia, Layout-Designs of Integrated Circuits Act 2000 (Act 601) Part V enables government use for public non-commercial purposes, explicitly including defense or internal security of Malaysia. All these ensure state access during critical times without outright expropriation.[37]

Impact of IC Layout Design Acts in Other Countries

China's 2001 ordinance protecting IPR for IC layout design helped spur the growth of domestic IC design companies. In 2024, a total of 11,000 IC layout design registrations and certificates were issued by China's National Intellectual Property Administration (CNIPA). By the end of 2024, China had issued a total of 83,000 IC layout-design certificates.[38] As foreign firms introduced more advanced process technologies into China, local companies acquired valuable production expertise that could propel their next technological leap.[39] In under a decade, China narrowed the gap in IC semiconductor processing from five generations behind to nearly matching state-of-the-art levels.[40] IC production sales in China surged from $2.72 billion in 2001 to $44.71 billion in 2010.[41] Thanks in part to strengthened IP protection, Western companies are now competing with one another to facilitate technology transfers to their Chinese partners.[42]

In India, in the landmark case M/S Puneet Industrial Controls vs. M/S Classic Electronics & Anr (2012), this case highlighted exactly why countries needed a dedicated IC layout law instead of relying on standard copyright or design acts. In the dispute, the plaintiff sued a competitor, claiming they had copied the unique electrical/electronic circuits and design layout printed on their circuit boards for electronic relay products.[43] The plaintiff initially brought the suit under the Copyright Act for copyright infringement and misappropriation of trade secrets.[44] The Delhi District Court rejected the plaint's framing under standard design/copyright law. The judge ruled that because these layouts consisted of transistors and circuitry elements designed to perform electronic functions, they fell squarely under the definition of a "semiconductor integrated circuit" and "layout design" under Sections 2(r) and 2(h) of the SICLDA, 2000.[45] Because copyright law cannot be claimed as a common-law right and must yield to specialized statutory regimes, the judge argued the suit under the Copyright Act was legally barred.[46] The case proved that in India, once a layout is applied to a commercial, functional component, you cannot protect it via standard copyright; you must seek remedy through the specialized sui generis semiconductor registry.

The Advancement of China

CNIPA released a draft amendment to the Regulations on the Protection of Integrated Circuit Layout Designs for public comment on Dec. 26, 2024. The Regulations on the Protection of Integrated Circuit Layout Designs (Revised Draft) were submitted to the State Council for review, set for further deliberation in 2026.

Some highlights of the Draft include:[47] China Article 4, Layout-designs created by foreigners, foreign enterprises, or other foreign organizations, if the

[36] Protection of Layout-Designs of Integrated Circuits Act, B.E. 2543 (2000). https://www.wipo.int/wipolex/en/legislation/details/3817

[37] Layout-Designs of Integrated Circuits Act 2000 (Act 601) (Malaysia). https://www.wipo.int/wipolex/en/legislation/details/3121

[38] "CNIPA Press Conference: Over 1 Million Invention Patents Granted in 2024." *China IP Law Update*, 15 Jan. 2025, www.chinaiplawupdate.com/2025/01/cnipa-press-conference-over-1-million-invention-patents-granted-in-2024/.

[39] Zhang, Yue, Jiang Yu, and Yanmei Liu. "Evolutionary dynamics of high technology industry: modeling of semiconductor sector in China." *Chinese Management Studies* 7.2 (2013): 200.

[40] ibid.

[41] Pecht, Michael G. "How China is closing the semiconductor technology gap." *IEEE Transactions on Components and Packaging Technologies* 27.3 (2004): 617.

[42] ibid.

[43] M/S Puneet Industrial Controls vs M/S Classic Electronics & Anr on 8 October, 2012.

[44] Kumar, Abhijeet, and Adrija Mishra. "Protecting trade secrets in India." The Journal of World Intellectual Property 18.6 (2015): 338.

[45] ibid.

[46] ibid.

[47] China National Intellectual Property Administration. (Dec.26, 2024). *CNIPA releases draft amendment to regulations on protection of integrated circuit layout*. The National Law Review.

country where the creators are from has signed an agreement on layout-design protection with China or has jointly participated in an international treaty on layout-design protection with China, shall enjoy exclusive rights to the layout-designs in accordance with these Regulations.

Foreigners must use a Chinese patent agency (Article 5), adhere to a good faith requirement (Article 9), benefit from restoration of rights (Article 11), and provide remuneration for creators (Article 17), while declaring originality to identify original parts of the design (Articles 24, 26); additionally, third parties may request reexamination of circuit layout designs (Article 32), with new damage calculations introducing punitive damages and a 5 million RMB cap for statutory damages (Article 46), alongside available evidence preservation (Article 47).

This commitment underscores a wider recognition among Chinese leaders of the need to protect innovations from infringement while fostering domestic advancement in technology-intensive sectors. These reforms aim not only to shield current inventions but also to spur future innovations throughout diverse industries. For entrepreneurs and companies doing business in or connected to China, such shifts may offer enhanced protection for their intellectual property and investments.

Comparative Table: IC Layout Design Acts in 11 Countries

This table summarizes differences across five categories of integrated circuit (IC) layout-design protection acts in the 11 countries analyzed in the comparative section. It is presented as a descriptive tool to facilitate visual comparison rather than as a quantitative analysis or frequency statistic. The presence or absence of any given characteristic reflects each country's specific legal, social, and trade context and should not be interpreted as indicating that a characteristic is more commonly used overall.

Category **Country**	**Definition**	**Reverse-engineering**	**Registration**	**Term**	**Reciprocal Protection**
Australia	Circuit Layouts Act 1989 (section 5) recognizes sui generis "eligible layout" as original circuit layout by eligible person or first exploited in Australia/eligible country, separate from other IP.	Permitted for private/research/teaching (aligned with TRIPS/IPIC).	Not required; automatic upon eligibility.	10 years from first commercial exploitation.	Yes, for eligible foreign countries.
Canada	Integrated Circuit Topography Act (section 2) establishes "topography" as the design of interconnections/elements for IC products, sui generis distinct from patents/copyrights.	Permitted for evaluation/analysis/research/teaching.	Required: application within 2 years of first exploitation.	Up to 10 years from filing or first exploitation (whichever earlier).	Yes, via international agreements.

https://natlawreview.com/article/cnipa-releases-draft-amendment-regulations-protection-integrated-circuit-layout

China	Regulations on the Protection of Layout-Designs of Integrated Circuits (Article 2) defines "layout-design" as three-dimensional disposition of elements/interconnections, sui generis protection.	Permitted for research/teaching (per IPIC/TRIPS).	Required with the State IP Office.	10 years from filing or first exploitation.	Yes, for foreigners from treaty countries or first exploited in China.
EU	Directive 87/54/EEC (Article 1) on legal protection of "topographies" of semiconductor products as series of images representing 3D pattern, sui generis regime.	Permitted for evaluation/analysis/research/teaching.	Optional in some states (within 2 years of exploitation).	10 years from first exploitation or filing; max 15 years from creation.	Via Directive transposition; reciprocal via agreements.
Hong Kong	Semiconductor Products (Protection of Topography) Ordinance recognizes "topography/layout-design" sui generis, aligned with the UK/EU model.	Permitted for permitted purposes (IPIC/TRIPS standard).	Required under Ordinance.	Typically 10 years.	Yes, designates qualifying countries/territories for reciprocity.
India	Layout Designs of Semiconductor Integrated Circuits Act, 2000 (section 2(h)) recognizes new IP category "layout designs" for semiconductor IC, separate from patents/copyrights/trademarks.	Permitted for analysis to create original designs.	Required with the Registrar.	10 years from filing or first exploitation.	Yes, per Act and treaties.
Japan	1985 Act on the Circuit Layout of a Semiconductor Integrated Circuits (Article 2) established "layout-design" as layout of circuitry elements/lead wires, sui generis "layout design licenses" separating from patents/copyrights/trademarks.	Permitted for research/compatibility (IPIC/TRIPS).	Required: registration of establishment.	10 years from first exploitation.	Yes, early adopter with reciprocity.

New Zealand	Integrated Circuit Layout Designs Act defines "layout design" as three-dimensional disposition of elements/interconnections of IC, sui generis protection.	Permitted for permitted acts (research etc.).	Not required: automatic.	10 years from first exploitation.	Yes, for eligible countries via agreements.
South Korea	Act on the Layout-Designs of Semiconductor Integrated Circuits (Article 2) defines "layout-design" as 2D/3D design of circuit elements/wires for semiconductor IC, sui generis	Permitted for reverse engineering/ research (standard).	Required (aligned with TRIPS).	10 years.	Yes, reciprocal with treaty nations.
Taiwan	Integrated Circuit Layout Protection Act (Article 2) defines "circuit layout" as a predetermined 2D/3D pattern of components/interconnecting leads on IC, sui generis.	Permitted for private/research.	Required; application for registration.	10 years from exploitation or filing.	Yes, if first exploited in Taiwan or home country reciprocates.
USA	Semiconductor Chip Protection Act of 1984 (17 USC. §901(a)(2)) creates sui generis "mask work" as a series of related images representing predetermined 3D patterns in semiconductor layers.	Permitted for research/teaching under SCPA exceptions.	Required; notice on products.	10 years from registration/ filing.	Yes, via SCPA and treaties.

Descriptions of the Integrated Circuit Layout Design Act in Vietnam

Definitions and Eligibility

Sui Generic Definition: "Integrated circuit" means a product, in final or intermediate form, with active elements and interconnections formed on material for electronic functions. "Layout design" (or topography) means the three-dimensional arrangement of such elements and connections, however expressed.

Eligibility: Protected if original, resulting from the creator's own intellectual effort and not commonplace among IC creators/manufacturers at creation time (no prior global exploitation). Applies regardless of incorporation into products, no novelty or inventiveness required.

Protected Subjects: Covers layout designs fixed in any form; excludes ideas, processes, or functional aspects alone.

Exclusive Rights

Scope of Rights: Right holders exclusively authorize:

(1) reproduction of the layout design by any means;
(2) commercial importation, sale, or distribution of the layout, IC incorporating it, or products containing such ICs.

This part will be a huge change and align with the new amendment of the IP Law and the Technology Transfer Law of Vietnam (Law No. 115/2025/QH15),. The amended IP Law contains changes aiming to transform Vietnamese research outcomes and inventions into assets that can be bought, sold and traded, moving toward an economy where IP comprises a significant portion, as in developed countries. The draft allows IPRs to be valued, traded and used as assets, marking a shift from mere protection to creating assets, commercialization and marketization of research results. IP becomes a strategic competitive tool for enterprises and the nation. The draft prioritizes purchasing IP rights related to important national security, socio-economic products, developing an IP ecosystem and encouraging investment in start-ups. Owners can determine value and asset lists for management if values are not yet recorded in accounting.

The amended Technology Transfer Law aims to complete the legal framework and promote effective, synchronous, and internationally aligned technology transfer activities. The amendment simplifies administrative procedures, updates the list of new and strategic technologies and widens incentives for transfer activities. It adds provisions on intermediary organizations for technology transfer, a common model abroad but lacking in Việt Nam, helping small enterprises and disadvantaged localities access and master new technologies. The draft also strengthens cross-border transfer control to ensure technology security and foster Vietnamese technology export.

Commercial Exploitation: Extends to any act for direct/indirect economic gain; rights independent of patents, copyrights, or designs.

Permitted Acts: No infringement for: private/non-commercial use; evaluation, analysis, research, or teaching (including reproduction), allow private use or exhaustion post-first sale.

Further Limits: Acts without right holder's knowledge not infringing if innocent; compulsory licenses possible for public interest per TRIPS.

Term of Protection

Duration: Minimum 10 years from: filing date, first commercial exploitation worldwide, or creation, non-renewable. Rights lapse earlier if layout enters public domain. The 15 years duration from creation in the current IP law in Vietnam is removed to be in line with international acts.

Registration System

Voluntary Registration: Applications to National Office of Intellectual Property (NOIP) within 2 years of first exploitation, includes samples, descriptions, and fees. No substantive examination beyond formalities.

Effects: Registration provides presumption of validity/originality publication in Official Gazette.

Foreign Applications: Priority via Paris Convention; automatic for treaty countries.

Enforcement and Remedies

Infringement: Civil actions for injunctions, damages (actual/profits), destruction of infringing goods. Administrative fines up to 500 million dong (around 19.000 US Dollar), criminal penalties for willful large-scale infringement.

Border Measures: Customs suspension of suspected imports. Provisional measures without owner disclosure.

Evidence: Registration shifts burden, reverse engineering defense requires proof.
Reciprocity and International Alignment

Treaty Compliance: Protection per TRIPS Articles 35–38 and IPIC Treaty (Articles 2–7, 12, 16(3)), treaty provisions prevail over conflicts. Nationals of WTO/Paris Convention members fully protected.

Reciprocity: Extend protection to foreigners from reciprocal nations.

Transitional and Final Provisions

Existing IP Law protections transition seamlessly. Effective 12 months post-enactment.

Competitive Edges for Vietnam

Innovation Incentives: Tax credits for R&D in IC design as seen in Circular 33/2025 outlines record-

setting corporate income tax (CIT) incentives for electronic equipment manufacturers in the Law on Digital Technology Industry (Law No. 71/2025/QH15) in June 2025. Effective from 01 January 2026. Fast-track registration to attract FDI in semiconductors. Ensuring export controls align with international dual-use regimes, mitigating risks from US BIS restrictions on Vietnam-related activities.

National Security Safeguards: Layout designs registered under this Act shall not be exploited or shared for military actions, defense purposes, or national security applications without explicit government authorization. Right holders must not disclose or transfer IC layout designs to third parties without verifying end-use compliance, including prohibitions on dual-use military applications.

A. Expansion with AI

During one of the meetings during the field trip as part of this program in the US Department of State in Washington DC with representatives from the Bureau of Cyberspace and Digital Policy and the Office of S&T Investment, Innovation, and Cooperation. The representative emphasizes that policymakers must closely track technological advances in academia to ensure regulatory frameworks are prepared prior to market deployment. Regulating intellectual property for AI in IC chip design is still in its early stages. However, when the IC Layout Design Act is under consideration, these IP issues must be addressed to guide further development.

The AI surge has generated vast opportunities for the semiconductor sector, encompassing both the provision of cutting-edge, AI-enabled chips and enhancements to chip design methodologies. Due to the high computational demands of AI algorithms, semiconductor producers have created specialized AI processors, also called AI chips or accelerators. AI chips are made to efficiently carry out tasks linked to AI, like inference and training of neural networks.[48] These prospects introduce multiple legal considerations that policymakers must address to secure value and sidestep disputes. The most evident concerns AI application in chip design, where training data origins and AI output ownership, key debates in Large Language Model (LLM) creation stand out. Second, considering the fast-evolving domain of AI-capable hardware, involving numerous players across various markets, questions about ownership of IPRs will change rapidly.

Protecting Chip Design IP in the Age of Generative AI

Adopting cutting-edge AI methods, like reinforcement learning, genetic algorithms, adversarial networks, and lately transformers sparks fresh concerns over their legal ramifications. While many approaches skip training data altogether or rely on proprietary sets, firms sourcing external data must scrutinize its origin and ownership. As extensively covered, OpenAI faces lawsuits from various parties alleging misuse of third-party copyrighted content. Semiconductor EDA and design firms must ensure their AI training data avoids third-party chip designs potentially protected by copyright or other IPR. Beyond that, companies should monitor third-party AI tools used by staff in design tasks. In 2022, Samsung banned certain LLMs after discovering employees inputting sensitive data into ChatGPT. Firms must also weigh AI's effects on IP ownership. In most jurisdictions, IP rights start with the employee and transfer to the employer via contract or statute. But if an AI process acts as the "inventor," who claims the IP? Courts largely agree only humans qualify as inventors. Thus, inventions from AI typically belong to the employees operating the systems. Still, this field evolves quickly, demanding vigilant oversight by policymakers.

AI Chip Co-Design: The Hardware–Software Intersection Reshaping IP Protection and Next-Generation IC Innovation

The convergence of software-like algorithms with physical chip design adds new layers of complexity to IP protection, creating tensions with current legal frameworks. The combined evolution of AI and IC technologies has driven major advances in the co-design of dedicated AI chips, improving performance, energy efficiency, and automation. A central element of this progress is the emergence of specialized hardware architectures tailored to AI workloads.

For instance, Google's Tensor Processing Unit (TPU) employs a multiplier-accumulator (MAC) array to

[48] Mukherjee, Sujit, Debmalya Pal, Arunava Bhattacharyya, Subhasis Roy. "Future of the semiconductor industry." Handbook of Semiconductors. CRC Press, 2024. 362.

accelerate demanding operations, such as convolutions in convolutional neural networks (CNNs). Through the parallel execution of large-scale matrix computations, MAC arrays dramatically cut processing time and improve energy utilization. Relative to conventional CPUs and GPUs, TPUs deliver roughly a 15–30× speedup and a 30–80× gain in energy efficiency, making them critical for real-time AI-driven design automation tasks, including layout optimization and simulation. [49] This architectural advance addresses the growing demand for high-throughput processing in contemporary IC design workflows.[50]

There's a current race to create AI-capable hardware for the next wave of AI applications. A key question is how specialized the chip should be. For instance, companies have previously built processors tailored for convolutional neural network architectures aimed at computer vision tasks, yet vision tasks are now often handled by vision transformers. Many top AI chips today prioritize transformers, the core architecture powering LLMs. Groq's language processing unit (LPU) stands out as one of the most specialized and high-performing options. In contrast, Nvidia's graphics processing units (GPUs) and Google's TPUs are more versatile, depending on low-level software like Nvidia's Compute Unified Device Architecture (CUDA) for optimal scheduling across architectures. That said, Nvidia's flagship chips (e.g., H100) are marketed as transformer engines. Major investments are pouring into transformers, but the field evolves quickly, and a new architecture could supplant them in certain areas. Plus, other models like diffusion models (common in image generators) might perform best on broader GPUs.

Beyond hardware acceleration, system-level optimizations play a vital role in surmounting bottlenecks that hinder computational efficiency. A key obstacle is the "memory wall," where memory bandwidth and latency constrain the full exploitation of processing power. To tackle this, specialized AI chips integrate high-bandwidth memory (HBM) and refined data flow architectures. HBM's stacked structure and broad interfaces enhance memory throughput, while streamlined data pipelines minimize unnecessary data movements between memory and processing units.[51] These enhancements facilitate seamless interplay between AI algorithms and hardware, supporting the effective rollout of demanding tools such as machine learning-based circuit optimizers. For example, in expansive IC designs, lower data latency enables iterative simulations to converge faster, accelerating design cycles and boosting productivity.[52]

The interplay between AI algorithms and IC hardware forms a bidirectional feedback loop that fosters advancements in both domains. AI-powered design tools harness the processing capabilities of specialized chips to iteratively optimize circuit layouts, forecast performance results, and automate parameter adjustments. In turn, hardware architectures evolve to accommodate new AI models, for instance by dynamically restructuring memory hierarchies to handle the vast data demands of deep learning or boosting parallelism for reinforcement learning-driven optimization. This mutual evolution tackles issues like non-linearity and fault tolerance, enabling scalable approaches for high-density, high-complexity IC designs. By integrating algorithmic intelligence with hardware strengths, the co-design approach guarantees that progress in AI and IC technology continually bolsters one another, propelling the creation of next-generation smart, energy-efficient electronic systems.[53]

The pace of development and the variety of companies engaged in chip design have arguably reached unprecedented levels. This situation prompts numerous questions regarding which technologies will ultimately prevail. At the heart of this competition lies ownership of critical IPR. Owing to the cross-border strategic significance of these matters, patent disputes in this field are likely to proliferate in the years ahead. Considering these challenges, companies prioritize safeguarding their interests through strategic patent filings and robust

[49] Goldie, Anna, Azalia Mirhoseini, and Jeff Dean. "That chip has sailed: A critique of unfounded skepticism around AI for chip design." *arXiv preprint arXiv:2411.10053* (2024).
[50] Maida, Payal, Yogesh Patidar, and M. P. Ujjain. (n 4)
[51] Wang, Zhihai, et al. "Benchmarking end-to-end performance of ai-based chip placement algorithms." *Advances in Neural Information Processing Systems* 38 (2026).
[52] Kang, Zhuowei. "Digital Integrated Circuit Design Automation Based on." *Proceedings of the 2025 2nd International Conference on Electrical Engineering and Intelligent Control (EEIC 2025)*. Springer Nature, 2025.
[53] Chen, Nuo. "Integrating AI into Semiconductor Design and Fabrication: Methodologies, Challenges and Future Prospects." *ITM Web of Conferences*. Vol. 78. EDP Sciences, 2025.

protection of trade secrets surrounding their essential technologies.

Limitations

The researcher recognizes the study's bias, limited time and word count necessitated concentrating on IC layout-design legislation in developed economies, resulting in less attention to the status of such acts in developing countries, even though Vietnam itself is a developing country and this research examined the IC layout design acts in some countries in Southeast Asia. It is important because one aim of this research is to show that enacting an IC layout-design law in Vietnam would strengthen the developing country's position in bilateral and multilateral dialogues and help align its chip-related legal framework with international norms.

Critics contend that international efforts to harmonize IP law have often resulted in developing countries adopting the higher protection standards of developed nations, sometimes through imposition rather than choice. These standards have, in many cases, set protection levels that were unnecessary or too stringent given the developmental stage of the receiving countries.[54] This process has also been criticized on the basis that it often benefits primarily large businesses operating internationally.[55] In the postcolonial perspective, the international IP system, particularly the TRIPS agreement, has reinforced colonial-era power relationships and limited the policy space of developing countries, leading to marginalization of the Global South.[56] This pattern has been evident historically and still persists in some cases. However, in recent decades, developed countries have also promoted certain limitations on IP rights, especially concerning copyright fair use. At the same time, as some developing countries' economies expand, their interest in IP laws has grown. Still, for international harmonization to be effective, it must allow enough flexibility to accommodate different national contexts and development levels, which can evolve over time.

Conclusion

Vietnam is emerging as a strategic player in the global semiconductor industry, yet its current IP framework lacks a dedicated, robust law for IC layout design. This gap discourages foreign investors who require clear, registered IP protections before committing to technology transfers. Vietnam must enact a standalone, comprehensive IC Layout Design Act, moving beyond the current generic "umbrella" of broader IP legislation. While Vietnam can learn from international models, simply copying foreign laws will not work. Instead, the country needs a targeted legal reform that adapts to current technological and market realities, leverages Vietnam's competitive advantages, and remains fully aligned with the IPIC Treaty and TRIPS Agreement framework. As AI-driven design automation and specialized hardware architectures reshape the semiconductor industry, Vietnam must proactively address the growing complexities of AI in IPR, ensuring that legal policies evolve in tandem with technological advancements. Policymakers should actively engage pioneers in both IP policy and chip design technology to help shape a forward-looking legal framework. By closing current legal gaps and aligning with international best practices, Vietnam can establish a secure, stable, and competitive environment for semiconductor innovation. This legal clarity will not only protect domestic creators but also incentivize the high-value international collaborations essential for Vietnam to succeed in the global semiconductor and AI race.

[54] Calboli, Irene. "Comparative legal analysis and intellectual property law: a guide for research." *Handbook of Intellectual Property Research* 609 (2021): 49.
[55] ibid.
[56] Khan, Bryan. "Intellectual property, development, and inclusiveness: A postcolonial critique." *Research Handbook on Intellectual Property Rights and Inclusivity*. Edward Elgar Publishing, 2024. 52.

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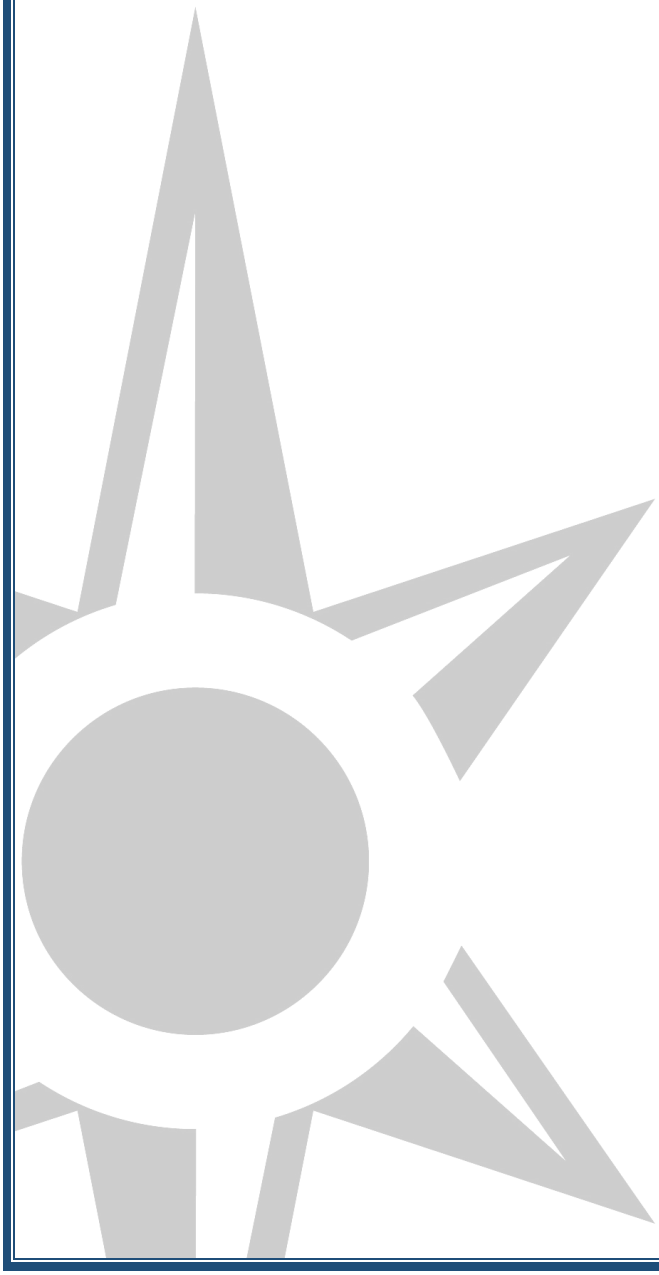
Vietnam in the Global AI and Semiconductor Value Chains: Opportunities and Challenges from Geopolitical Competition and Export Control Measures

By
Tuyet Tran (Snow)



Executive Summary

Tuyet Tran (Snow)

The global semiconductor landscape is undergoing a fundamental transformation as technological ordering shifts from cost-optimization to security-driven logic, with chips becoming geopolitical leverage rather than purely industrial inputs. Concurrently, frontier AI is magnifying semiconductor bottlenecks and transforming chips into core digital power infrastructure, while Indo-Pacific supply chain restructuring through friend-shoring creates narrow windows for new trusted nodes. This research examines Vietnam's position in the AI semiconductor value chain and analyzes how these converging forces affect its strategic opportunities. Using mixed-methods analysis, the study maps Vietnam's capabilities across upstream, midstream, and downstream segments of the AI and chip ecosystem through systematic value chain analysis and export controls impact assessment.

Vietnam's semiconductor landscape, shaped by investments from Intel, Samsung, and Amkor, is at a critical juncture where geopolitical shifts and export control measures shape multiple scenarios for strategic policy choices and targeted development approaches in the AI and semiconductor ecosystem specifically, and national semiconductor strategy more broadly. The research identifies strategic positioning options, examines gaps in Vietnam’s existing export control framework, and provides evidence-based recommendations to strengthen these mechanisms. It offers policy pathways for Vietnam to leverage these geopolitical shifts and find its strategic niche in the AI semiconductor value chain, balancing between competing technological ecosystems while building indigenous capabilities in specialized areas.

Introduction

For more than three decades, the global semiconductor industry operated on David Ricardo's theory of comparative advantage, where cost efficiency and geographic specialization of supply chains were top priorities. Chris Miller, in *Chip War: The Fight for the World's Most Critical Technology*, argues that the industry's structure was built to optimize efficiency. Historically, the United States led in chip design, drawing on its strong base of intellectual capital and innovation. Taiwan and South Korea dominated fabrication, backed by advanced manufacturing technology and highly efficient production at scale. Meanwhile, Southeast Asian economies, including Vietnam, established a foothold in the packaging and assembly segment, supported by a competitive and growing workforce. As the second half of the 2020s unfolds, however, this long-standing division of labor has been undergoing a profound transformation.

Underpinning this structure was Moore's Law, with the expectation that transistor density would double roughly every two years. Yet as chip geometries approach physical limits at 2nm and below, the pace of miniaturization is slowing.[1] This inflection point creates an innovation drought for incumbents and, paradoxically, a window of opportunity for late-entrant economies to build competitive capacity before the next technological order solidifies. Unlike the 2nm race, emerging paradigms such as 3D stacking, advanced packaging, and neuromorphic computing demand a different set of capabilities. The question for ambitious late-entrant economies is not whether to enter the semiconductor industry, but whether they can move up the value chain fast enough to claim a position in the next paradigm before new incumbents emerge. This long-standing division of labor is now being fundamentally renegotiated. The second half of the 2020s marks a turning point, one driven by geopolitics as much as by technology.

According to Farrell & Newman (2019),[2] the world is entering an era of "weaponized interdependence," in which technological, financial, and infrastructural chokepoints are transformed into instruments of geopolitical coercion. Semiconductors are no longer an ordinary industrial input; they have become the refineries of the 21st century. If data is the new oil, semiconductors are the infrastructure that makes it flow. The United States' enactment of the CHIPS and Science Act (2022), alongside stringent export controls issued by the Bureau of Industry and Security (BIS) updated in 2025, established a new reality: technology is power. Nations no longer seek the cost-efficient source of supply; they are seeking the most secure and trusted one. The shift from global value chains to trusted value chains represents a structural disruption that every emerging economy, Vietnam included, must now confront.

This geopolitical shift is amplified by the rise of Frontier AI. As the world transitions from Generative AI (GenAI) to Agentic AI in 2025 and 2026, the strategic importance of semiconductors, long the core infrastructure of digital power, has only intensified. The US Semiconductor Industry Association (SIA) reported on Feb. 6 that global semiconductor industry revenue reached US$791.7 billion in 2025, a growth of 25.6% compared to the $630.5 billion recorded the previous year[3]. Deloitte also projects that the global semiconductor industry is expected to reach annual revenue of $975 billion in 2026, a historic peak driven by the strong surge in AI infrastructure investment. Within this landscape, high-value AI chips now drive roughly half of total revenue, yet they represent less than 0.2% of total unit volume.[4] AI has created a scarcity paradox: demand for computing capacity doubles every five months,[5] while access to advanced manufacturing processes

[1] Zhang, Q. & Deng, H. & Song, K.. (2025). *Breaking Physics Limits: How 2nm Chip Technology Powers Next-Gen 3D ICs.* Fusion of Multidisciplinary Research, An International Journal. 6. 685-706. 10.63995/BRIT1756.

[2] Farrell, H., & Newman, A. L. (2019). *Weaponized Interdependence: How Global Economic Networks Shape State Coercion.* International Security, 44(1), 42–79. https://doi.org/10.1162/ISEC_a_00351.

[3] Semiconductor Industry Association. (2026). *Global Annual Semiconductor Sales Increase 25.6% to $791.7 Billion in 2025.* https://www.semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025/.

[4] Kusters, J., Stewart, D., Ramachandran, K., Bish, J., & Bhattacharjee, D. (2026). *2026 Global Semiconductor Industry Outlook.* Deloitte. https://www.deloitte.com/us/en/insights/industry/technology/technology-media-telecom-outlooks/semiconductor-industry-outlook.html.

[5] Maslej, N., Fattorini, L., Perrault, R., Gil, Y., Parli, V., Kariuki, N., Capstick, E., Reuel, A., Brynjolfsson, E., Etchemendy, J., Ligett, K., Lyons, T., Manyika, J., Niebles, J. C., Shoham, Y., Wald, R., Walsh, T., Hamrah, A., Santarlasci, L., ... Oak, S. (2025). The AI Index 2025 Annual Report. AI Index Steering Committee, Institute for Human-Centered

below 5nm is increasingly constrained by political barriers. For Vietnam, this means that participation in the semiconductor value chain is no longer a purely economic choice; it is a prerequisite for not being left behind in the global digital infrastructure revolution.

Vietnam at the Center of the Indo-Pacific "Window of Opportunity"

The Indo-Pacific region is undergoing deep restructuring through friend-shoring strategies. This shift is no longer simply a "China + 1" dynamic,[6] it has become a search for new trusted nodes. Vietnam has emerged as a strong candidate through the convergence of three factors: political stability, strategic geographic positioning, and an existing electronics manufacturing base. Statistics from early 2026 bear witness to this trajectory:

- Foreign Direct Investment (FDI): Total investment in the semiconductor sector has reached 11.6 billion USD, with the presence of industry giants such as Intel (the world's largest ATP facility in Ho Chi Minh City), Amkor (a $1.6 billion project in Bac Ninh focused on advanced packaging for AI chips), and Samsung (with the largest R&D center in Southeast Asia).
- Upstream Shift: In early 2026, Viettel Group broke ground on Vietnam's first chip fabrication facility operating at a 32nm process node at the Hoa Lac Hi-Tech Park, with pilot production expected to begin in 2028. This marks Vietnam's first step into the Midstream (fabrication) segment.
- Strategic Cooperation: The United States' consideration of removing Vietnam from its strategic export control list (February 2026) opens opportunities for Vietnam to access high-end EDA tools and chip design software from Synopsys and Cadence.

While the potential is substantial, this study argues that Vietnam's position faces serious structural bottlenecks. Vietnam remains largely in the downstream segment (packaging and testing), where value-added is lower and the risk of substitution is higher.

- Workforce Shortage: Although Decision 1018/QD-TTg[7] sets a target of training 50,000 engineers by 2030, Vietnam currently has only around 15,000 professionals with sufficient competency to work within the semiconductor ecosystem, of whom only approximately 7,000 are IC design engineers. The gap between political targets and actual training capacity creates a risk of quality dilution within the talent pool. Recent Vietnam–US cooperation in high-tech industries and the shared commitment of government, academia, and industry to build the next generation of semiconductor talent have been gaining significant attention (e.g. Arizona State University's MoU with the city of Hanoi to advance cooperation in semiconductor education, research, and workforce development).[8]
- Legal Gap in Export Controls: This is a weakness that receives little discussion yet carries decisive consequences. To become a trusted node in the US and Western supply chains, Vietnam needs an export control legal framework that meets international standards, such as those set by the Wassenaar Arrangement. Without such a mechanism, core technologies will never be transferred, due to the risk of technology leakage to competing parties.
- Strategic Ambiguity: Vietnam's current policies tend to focus on broad-based FDI attraction without identifying a specific strategic niche. The absence of quantitative targets and detailed enforcement measures

AI, Stanford University. https://doi.org/10.48550/arXiv.2504.07139.

[6] Source of Asia. (2022). *China Plus One Strategy in ASEAN: Why Vietnam Stands Out.* https://www.sourceofasia.com/china-plus-one-strategy-vietnam/.

[7] Prime Minister of Vietnam. (2024). *Decision No. 1018/QD-TTg on Promulgating the Strategy for development of Vietnam's semiconductor industry through 2030, with a vision toward 2050.* LuatVietnam. https://english.luatvietnam.vn/cong-nghiep/decision-1018-qd-ttg-2024-strategy-for-development-of-vietnams-semiconductor-industry-through-2030-366694-d1.html.

[8] Arizona State University. (2026). *Arizona State University and City of Ha Noi Sign Landmark Memorandum of Understanding to Advance Semiconductor Education, Research, and Workforce Development.* https://asuengineeringonline.com/content/arizona-state-university-and-city-ha-noi-sign-landmark-memorandum-understanding-advance.

means that policy outcomes frequently fall short of expectations.

Research Objectives and Paper Structure

This research focuses on identifying an optimal strategic position for Vietnam within the AI semiconductor value chain, which is being reshaped by geopolitical forces. Drawing on systematic value chain analysis and export control impact assessment, this study will:

- Map Vietnam's actual capabilities across three segments: Upstream (Design), Midstream (Fabrication), and Downstream (ATP).
- Analyze how various US-China competition scenarios affect Vietnam's policy option space.
- Provide recommendations for strengthening the export control legal framework to improve Vietnam's national trust.

Based on these analyses, this study aims to offer an evidence-based policy roadmap that enables Vietnam not only to leverage geopolitical shifts to attract capital, but also to build sustainable indigenous capabilities in specialized fields, securing its position as an indispensable strategic node in the semiconductor map of the future.

I. Vietnam's Position in the AI Semiconductor Value Chain

Value Chain Mapping: Where Does Vietnam Stand?

Vietnam's position in the global semiconductor value chain is undergoing a powerful reshaping process, transitioning from a low-end outsourcing destination to a highly specialized link within the high-tech supply chain structure. When viewed through the Global Value Chain (GVC) analytical framework for the semiconductor industry, the domestic ecosystem is forming an uneven yet strategically oriented development structure, in which breakthroughs at both ends of the value chain, namely design (upstream) and assembly, testing and packaging (downstream), partially compensate for the significant gap in wafer fabrication (midstream). This development model reflects a common trend among emerging economies in the semiconductor sector, where entry into the value chain does not necessarily begin at the core manufacturing stage, but can instead occur through segments that offer advantages in human capital, cost, and the ability to integrate into global production networks.

In the Upstream segment, Vietnam has gradually built a notable chip design workforce of over 5,600 design engineers working at R&D centers of multinational corporations.[9] Companies such as Marvell Technology, Synopsys, and Cadence Design Systems have established research and design centers in Vietnam, making the country an important destination within the global chip design network. The presence of these centers not only helps train a highly skilled engineering workforce but also generates knowledge spillovers into the broader domestic technology ecosystem.

However, a key characteristic of the current development phase is that the majority of value-added in design activities still resides within design service models, meaning the provision of design services on demand for global corporations, rather than the development of independently owned chip architectures. Domestic enterprises such as FPT Semiconductor and Viettel Group have taken initial steps toward commercializing power management ICs and chips for telecommunications infrastructure. Nevertheless, they remain significantly dependent on IP libraries and design tools from international vendors. This reflects a common reality in the global semiconductor industry: technological power and the highest profits continue to concentrate among firms that own core IP and chip architectures, particularly in fast-growing fields such as AI chips and data center processing. In this context, Vietnam currently plays the role of an important design talent incubator for the global market, rather than an independent hub for chip architecture innovation.

In contrast, in the downstream segment, covering Assembly, Testing and Packaging (ATP), Vietnam has built a clear and increasingly reinforced competitive advantage. The presence of Intel, with its Intel Products Vietnam facility in Ho Chi Minh City, currently the largest packaging and testing facility in

[9] Information and Statistics Agency. (2025). *Workshop on Developing Policies and Solutions to Promote the Development of Vietnam's Semiconductor Industry.* Information Portal of the Information and Statistics Agency, Ministry of Science and Technology. https://vista.gov.vn/vi/news/chien-luoc-chinh-sach-kh-cn-dmst/hoi-thao-xay-dung-chinh-sach-va-giai-phap-thuc-day-phat-trien-nganh-cong-nghiep-ban-dan-viet-nam-12527.html.

the corporation's global network, has laid the foundation for Vietnam's ATP capabilities. In addition, Amkor Technology's $1.6 billion investment in Bac Ninh marked an important turning point as Vietnam began entering the field of Advanced Packaging.[10]

As the global semiconductor industry enters the post-Moore's Law era,[11] advanced packaging technology is emerging as a key solution for increasing computational performance. Architectures such as chiplets, 2.5D packaging, and 3D stacking allow multiple specialized chips to be integrated into a high-performance processing system without full dependence on ultra-fine manufacturing processes. In this context, ATP capability is no longer merely a low-value stage in the production chain; it is becoming a technologically strategic node of major importance. Projections by the Semiconductor Industry Association (SIA) and BCG that Vietnam will grow strongly in the ATP segment, rising from a 1% global market share in 2022 to 8% by 2032,[12] indicate that the country is gradually becoming an important downstream node in the Asia-Pacific semiconductor supply chain.

Nevertheless, the Midstream segment, covering wafer fabrication at chip foundries (fabs), remains the largest weakness in Vietnam's semiconductor capability structure. Building a modern semiconductor fab requires investment of between $10 and $20 billion, along with an extremely complex equipment and materials supply chain that includes advanced lithography systems from ASML. This segment is also subject to strict Western technology export control policies, particularly amid intensifying global strategic technology competition. These factors have led many developing economies, including Vietnam, to adopt a fab-light strategy, focusing on design and packaging rather than directly investing in advanced wafer manufacturing.

Within this context, Viettel Group's semiconductor facility project at the Hoa Lac Hi-Tech Park, launched in 2026, has significant strategic importance. The project targets mastery of manufacturing processes at the 28 to 32nm range. These are considered mature nodes, which continue to play an important role in fields such as telecommunications, IoT devices, defense systems, and digital infrastructure. This approach reflects a pragmatic development strategy: rather than racing in the cutting-edge technology segment with its high financial and political risks, Vietnam prioritizes building specialized chip manufacturing capabilities to serve domestic needs and strategic applications.

National Policy Architecture: SET + 1 Strategic Framework

The SET + 1 strategic framework[13] can be understood as a form of selective industrial policy, in which Vietnam proactively identifies value chain segments where effective participation is feasible, rather than pursuing a strategy of comprehensive self-sufficiency. In the semiconductor industry, an ecosystem characterized by high specialization and fragmentation, this approach reflects strategic niche integration, seeking entry points where comparative advantages exist.

At its core, the formula C = SET + 1 is not merely a policy slogan but a strategic structure designed to synchronize three endogenous factors (Specialization, Electronics ecosystem, Talent) with an exogenous geopolitical variable (+1, representing national positioning). This indicates that Vietnam is approaching the semiconductor industry not simply as a new industrial field, but as a pillar of its national technology security strategy amid increasingly intense global supply chain competition.

S (Specialization): Selecting a Niche Position Within the Value Chain

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[10] Amkor Technology. (2023). *Amkor Inaugurates Latest Factory in Vietnam.* https://amkor.com/blog/amkor-inaugurates-latest-factory-in-vietnam/.

[11] Further transistor miniaturization is becoming increasingly difficult both physically and financially.

[12] Varadarajan, R., Koch-Weser, I., Richard, C., Fitzgerald, J., Singh, J., Thornton, M., Casanova, R., & Isaacs, D. (2024). *Emerging Resilience in the Semiconductor Supply Chain.* Boston Consulting Group & Semiconductor Industry Association. https://www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf.

[13] Prime Minister of Vietnam. (2024). *Decision No. 1018/QD-TTg on Promulgating the Strategy for development of Vietnam's semiconductor industry through 2030, with a vision toward 2050.* LuatVietnam. https://english.luatvietnam.vn/cong-nghiep/decision-1018-qd-ttg-2024-strategy-for-development-of-vietnams-semiconductor-industry-through-2030-366694-d1.html.

The Specialization pillar reflects the strategic recognition that Vietnam cannot compete directly in the General-Purpose CPU segment, a field dominated by corporations such as Intel, Advanced Micro Devices (AMD), and NVIDIA. These chip lines require R&D expenditures of tens of billions of US dollars and depend on advanced manufacturing processes below 5nm. Instead, Vietnam's strategy focuses on Application-Specific Integrated Circuits (ASICs) and specialized chips serving specific technology ecosystems. Priority segments include:

- AI chips for Edge Computing: low-power AI accelerators for smart cameras, low-level autonomous vehicles, and industrial IoT devices.
- IoT and sensor chips serving smart city systems and Industry 4.0 applications.
- Power Management ICs (PMICs) for consumer electronics and telecommunications infrastructure.

A common characteristic of these segments is that they can be manufactured on mature nodes (28nm to 90nm), which are significantly less costly than advanced process nodes. This allows Vietnamese companies to participate in the value chain without investing in extremely expensive fabs like those of TSMC or Samsung Electronics. Furthermore, the surge of Edge AI across fields such as smart home appliances, surveillance cameras, and industrial automation systems is creating a new market where mid-sized companies can still compete. This is the strategic window that Vietnam's specialization policy is seeking to exploit. However, this assessment of the strategic window requires a more candid examination on three points.

First, low barriers to entry set off a downward spiral of competition. Because mature nodes require relatively modest capital investment and face fewer export restrictions, they have become the most intensely contested segment of the semiconductor market—and competition in this space does not follow conventional market logic. When some actors are able to expand capacity beyond demand through extensive state support, price wars are not merely a risk but an almost inevitable outcome.

In the standard IoT chip segment, one of the primary targets of Pillar S, average selling prices have declined sharply in recent years, driven in part by a wave of excess capacity entering the market. As a result, margins in this segment are structurally thin, particularly for firms without proprietary design IP, leaving them highly vulnerable to fluctuations in input costs and exchange rates. Within such a structure, Vietnam cannot compete on cost alone. If a specialization strategy cannot clearly answer the question of "compete on what, if not price?", then the argument for mature nodes as an entry advantage needs to be fundamentally reconsidered.

The only economically viable pathway is to move from commodity chips toward differentiated products, those incorporating proprietary design IP and optimized for specific applications to the extent that customers cannot easily substitute them with standard alternatives. Yet this is precisely the capability Vietnam currently lacks at sufficient scale.

Second, the pressure of price competition feeds directly into a technological catch-up trap. To escape price wars in commodity segments, the logical pathway is continuously upgrading: moving from standard chips to application-specific designs, from contract-based design to proprietary IP, and from older to more advanced process nodes. Yet this is a race in which the gap with the technological frontier does not automatically narrow, for two structural reasons.

(i) Incumbent foundries operating at mature nodes have accumulated over a decade of learning effects. Their production costs continue to decline over time through process optimization, yield improvement, and economies of scale, while late entrants must absorb high initial costs without the benefit of comparable experience. This creates a persistent cost asymmetry that is difficult to overcome through incremental upgrading alone.

(ii) The application lifecycle in target segments is evolving faster than expected. Emerging generations of IoT devices and industrial systems are increasingly integrating on-device AI capabilities, raising performance and energy-efficiency requirements beyond what older nodes can efficiently deliver. As a result, by the time late entrants fully develop capabilities at a given node, market demand may already be shifting toward more advanced technologies supplied by incumbents with deeper capabilities and declining cost structures.

This dynamic constitutes a "reinventing the wheel" trap, as resources are invested to master a technology

just as its market relevance begins to erode. The problem is further compounded by the sunk-cost nature of semiconductor manufacturing. Once fabrication facilities are built, strong political and economic pressures, ranging from employment protection to the need to justify public investment, make it difficult to scale down or exit, even under persistently low or negative margins.

Third, even if the first two traps are avoided, the challenge of achieving sufficient output scale remains for Pillar S. Suppose Vietnam successfully identifies a niche segment of application-specific chips that aligns with the strategic objectives of Pillar S and is insulated from price wars and catch-up traps. Even then, developing a specialized ASIC line, covering design, verification, and production preparation, requires substantial upfront investment. Recovering these costs depends on securing long-term orders from anchor customers before production begins.
Fabless companies in Taiwan and Israel have thrived because decades of accumulated relationships provide the confidence to commit to large-scale production. In Vietnam, the domestic market remains too small to serve as an anchor for Pillar S initiatives, and there are no mechanisms encouraging multinational corporations to source preferentially from local suppliers. Without such foundational market support, Vietnamese firms risk facing a persistent gap between technological capability and economic viability.

E (Electronics Ecosystem): Leveraging the Export Electronics Industry

The Electronics pillar reflects an approach centered on leveraging the existing industrial ecosystem. Vietnam is one of the world's largest electronics manufacturing hubs, with electronics and components export turnover reaching hundreds of billions of US dollars annually. Corporations such as Samsung Electronics, Apple, LG Electronics, and Foxconn have established large production facilities in Vietnam.

The presence of these corporations creates a captive market, meaning a readily available domestic consumption market for electronic components, including semiconductor chips. In global value chain theory, this is an important driver of industrial upgrading, as domestic enterprises can progressively integrate into the supply chains of multinational corporations. However, global corporations such as Samsung, Apple, and Foxconn operate within buyer-driven global value chains, where decisions to purchase components, including chips, are made at the corporate level, not at local factory sites. The chip supply chain for Samsung in Bắc Ninh, for example, is integrated into the global procurement system of Samsung Electronics in Seoul, with pre-approved suppliers meeting highly stringent technical standards and quality inspections.

For a Vietnamese chip company to become a supplier to these corporations, it is not enough to produce chips that meet specifications, they must also navigate a supplier approval process that can take 18 to 36 months, demonstrate stable production capacity at the scale of millions of units, and comply with supply-chain audit requirements that most domestic firms currently lack the systems to fulfill. A captive market only becomes a genuine opportunity once domestic firms surpass this minimum capability threshold, and this threshold is significantly higher than what current policy implicitly assumes.

The deeper challenge is that multinational corporations are only incentivized to integrate local suppliers into their chains when the cost of sourcing internationally is high enough to justify the investment in developing local suppliers. With global supply chains already optimized over decades, this threshold has not yet been reached for most semiconductor components. Empirical evidence supports this concern: even after more than twenty years of large-scale electronics FDI, the localization rate within Vietnam's electronics supply chains remains low, indicating that enclave economies are more the rule than the exception.

One positive point is that the electronics ecosystem provides three strategic benefits: technology spillovers from global manufacturers to domestic enterprises; stable market demand for specialized chips designed by local companies; and the formation of industrial clusters in areas such as Bac Ninh, Thai Nguyen, and Ho Chi Minh City. In these clusters, semiconductor R&D, manufacturing, and packaging activities can be integrated with the existing electronics supply chain, if companies conduct proper due diligence and clearly define customer and end-user requirements.

However, upon closer inspection, industrial clusters constitute a necessary, yet insufficient, condition. Geographic concentration is often cited as evidence

of a maturing ecosystem; yet, high geographic density does not equate to high density of linkages. Most factories within the same industrial park currently operate as largely self-contained units, each with its own supply chain and internal processes, without sharing specialized labor or tacit knowledge in ways that generate true network effects. To transform these clusters into a cumulative advantage for Vietnam's domestic semiconductor industry, proactive connectivity mechanisms are needed. These could include structured supplier development programs with binding commitments, as well as shared R&D centers that facilitate knowledge exchange and collaboration, elements that current policy frameworks have not yet fully designed or implemented.

T (Talent): Human Capital as a Strategic Resource

The Talent pillar is the core foundation of Vietnam's semiconductor strategy. In the semiconductor industry, highly skilled personnel, particularly chip design engineers and system architects, are the decisive factor in value chain participation capability. Through Decision 1017/QD-TTg,[14] the Government targets the training of 50,000 semiconductor engineers by 2030. This is an ambitious goal relative to the current baseline, as Vietnam had only around 7,000 people working in packaging, testing, materials, and semiconductor equipment as of 2026.

To support this target, Vietnam has established 18 universities and four shared semiconductor laboratories across Hanoi, Danang, and Ho Chi Minh City. The Ministry of Education and Training has standardized curricula for 38 undergraduate and 37 master's programs related to microelectronics, laying the groundwork for the 2026 enrollment cycle. Early enrollment figures from 2025 suggest strong initial uptake, with over 137,000 students registered in semiconductor-related programs.

Yet enrollment numbers tell only part of the story. In 2025, the actual number of Vietnamese engineers gaining practical semiconductor design experience increased by only about 1,000, primarily through upskilling engineers from adjacent fields rather than through new graduates entering the workforce. This gap highlights the challenge of translating theoretical training into industry-ready skills.

The core challenge lies not in quantity but in workforce quality. Effective participation in chip design value chains and the creation of proprietary IP requires mastery across multiple layers of capability. Front-end design includes RTL coding, functional simulation, and logic verification. Back-end design includes physical layout, timing closure, and sign-off. Tape-out translates logical designs into manufacturable flows using a foundry-specific Process Design Kit or PDK. These layers are interdependent, and practical understanding emerges most fully when students experience the complete cycle from specification to silicon.

Vietnamese universities have made strong progress on front-end digital design through partnerships with Cadence and Synopsys. Complementing this with a lab-to-fab model, where students can test designs on packaging lines or through Multi-Project Wafer programs, is considered decisive for bridging theoretical knowledge and practical engineering skills. This approach aligns with the chip segments targeted under Pillar S. However, access to commercial PDKs remains limited, constraining students' exposure to end-to-end tape-out processes. While graduates can design functional chips in software, opportunities to fabricate these designs on commercial nodes remain limited.

A key policy question emerges. Does the current training system sufficiently align with the needs of Pillars S and E? Pillar S requires engineers capable of designing specialized ASICs with indigenous IP, including practical tape-out skills. Pillar E requires engineers able to integrate into multinational supply chains, understanding quality standards and design verification processes demanded by major foundries and customers. Both objectives remain constrained by the gap between classroom-based training and hands-on industry exposure, and by the limited integration between universities and the semiconductor market. This disconnect represents not just a technological gap but a skills gap between higher education and industry needs.

[14] Prime Minister of Vietnam. (2024). *Decision 1017/QD-TTg 2024 on Program on Development of Human Resources for the Semiconductor Industry through 2030.* LuatVietnam. https://english.luatvietnam.vn/cong-nghiep/decision-1017-qd-ttg-2024-program-on-development-of-human-resources-for-the-semiconductor-industry-through-2030-366646-d1.html.

+1 (Vietnam): The Geopolitical Variable and the Trusted Node Strategy

The +1" component in the SET + 1 formula represents the geopolitical factor, an increasingly important variable in the global semiconductor supply chain. Following supply chain shocks during the 2020 to 2023 period, many countries and technology corporations deployed friend-shoring and China+1 strategies to reduce dependence on single manufacturing centers. Vietnam is positioning itself as a trusted node, a stable and reliable transit point within the global technology network. Vietnam's advantages within this strategy include political stability, a long-term investment environment, balanced relationships with multiple major technology blocs, and competitive operating costs compared to established manufacturing centers such as Malaysia and Singapore. Driven by these factors, Vietnam is becoming a backup node in the regional semiconductor supply chain, complementing primary manufacturing centers such as Taiwan, South Korea, and China. This role is particularly significant as global technology corporations seek to diversify geopolitical risk.

SET + 1 demonstrates that Vietnam is pursuing a pragmatic and strategically oriented semiconductor strategy, rather than chasing the ambition of comprehensive self-sufficiency as some other countries have done. This strategy rests on three core principles: participating in the value chain through segments offering comparative advantages (design and packaging); leveraging the existing electronics industrial ecosystem to generate market demand; and promoting technology spillovers.

Vietnam's emerging position as a trusted node is shaped not by diplomatic logic but by legal logic, specifically US and allied export control requirements. Strategic neutrality does not automatically provide value. Instead, it represents a legal gray zone that US technology companies cannot accept when transferring sensitive technologies. A US firm seeking to transfer advanced EDA tools or proprietary chip IP to a Vietnamese partner requires not only political will but legal assurance that Vietnam has an export control framework robust enough to prevent technology from reaching sanctioned entities. Without such assurance, Vietnam's neutrality becomes a reason for Western technology partners to limit engagement to assembly-level FDI rather than full technology transfer.

Decree 259/2025/ND-CP is a step in the right direction but must be assessed in context. It is Vietnam's first legal instrument addressing the control of strategic goods at a level comparable to international standards. The gap between this first decree and a fully operational export control system recognized by the Wassenaar Arrangement involves years of implementation, institutional capacity building, and demonstration of compliance and track record. Policy statements alone cannot bridge this gap. Meanwhile, regional competitors such as Malaysia and Singapore have more mature export control systems, creating institutional advantages that Vietnam cannot close in the short term.

A frequently overlooked dimension of Vietnam's geopolitical position is the asymmetric dependency emerging in its semiconductor supply chain. Vietnam relies on Western countries for technology and design software while simultaneously depending on China for specialized materials and chemicals for advanced packaging and testing segments. Under normal conditions, these dependencies may balance each other. However, during heightened US-China tension, both dependencies could be constrained simultaneously. The US could tighten access to critical technologies while China restricts materials. Vietnam would have limited leverage to negotiate, and companies such as Intel or Samsung operating in the country would face these risks independently, a situation no investor likes when planning long-term capital commitments.

This explains why Vietnam's current positioning as a backup node provides value only under contingency scenarios. A backup node is activated when a primary node is disrupted, not because it possesses intrinsic competitive advantages. If Vietnam stops at this positioning without creating reasons for customers to choose the country even under normal circumstances, through switching costs, proprietary IP, or irreplaceable capabilities, its status as a trusted node will remain contingent on external geopolitical instability rather than on domestic strengths.

Vietnam's Strategic Pathways in the Semiconductor Value Chain

Scenario Construction: Key Assumptions and Variable Drivers

Several structural conditions are treated as invariant across the five scenarios, which will be presented below, because they reflect durable features of Vietnam's position that are unlikely to change materially within the 2025 to 2030 analytical horizon regardless of policy choices.

Vietnam's geographic position and political stability are treated as fixed advantages. The country's location within the Indo-Pacific supply chain restructuring zone, its relatively stable governance environment, and its existing bilateral relationships with both the United States and China are assumed to persist across all scenarios. These are not conditions that any of the five scenarios creates or destroys, they are the baseline endowment that all scenarios build upon.

The presence of anchor FDI in the electronics and semiconductor ecosystem is treated as fixed. Intel's packaging and test operations, Samsung's electronics manufacturing complex, and Amkor's committed investment in advanced packaging capacity are assumed to remain operational across all scenarios. These investments are too large, too operationally embedded, and too strategically significant to their owners to be reversed within the analytical horizon, and their presence defines the minimum capability floor below which no scenario operates.

The structural direction of US-China technology competition is treated as fixed. All five scenarios assume that the geopolitical pressure driving friend-shoring and trusted supply chain development continues at roughly its current intensity through 2030. The policy instruments through which this competition is expressed, including specific BIS rules, Wassenaar discussions, and Chinese material controls, are treated as variable, but the underlying dynamic that makes Vietnam's positioning relevant is assumed to persist.

The fundamental structure of Vietnam's domestic semiconductor ecosystem, specifically its concentration in downstream ATP with emerging upstream design capability and absent midstream fabrication, is treated as the starting condition from which all scenarios diverge. No scenario assumes that Vietnam begins from a more advanced position than it actually occupies.

The divergence between the five scenarios is generated by variation in four drivers, each of which can take different values depending on the policy choices Vietnam makes and the responses those choices elicit from partner countries and technology suppliers.

The first variable driver is the degree of synchronization across the SET+1 pillars. The SET+1 framework identifies four interdependent conditions for semiconductor value chain participation, but nothing guarantees that they develop at the same pace or in a mutually reinforcing direction. Scenarios diverge partly based on whether S, E, T, and +1 develop in coordination, producing compounding returns, or develop independently, producing fragmented progress that does not accumulate into system-level capability. Scenario 0 represents maximum desynchronization. Scenarios 2, 3, and 4 represent progressively higher degrees of pillar synchronization in different combinations.

The second variable driver is the speed and credibility of Vietnam's domestic export control compliance infrastructure development. This driver directly shapes what technology flows are permitted, at what cost, and with what degree of reliability across all four control regimes. A Vietnam that builds credible compliance infrastructure quickly unlocks technology access pathways that a Vietnam with slow or superficial compliance development cannot. This driver varies across scenarios from minimal development, as in Scenario 0, to sufficient development to support VEU certification and bilateral recognition, as in Scenarios 2 and 3, to the sustained multi-jurisdiction compliance management that Scenario 4 requires.

The third variable driver is the extent to which indigenous IP generation capacity develops within the domestic chip design ecosystem. This driver is primarily a function of the T pillar, specifically the quality rather than quantity of engineering talent development, combined with the technology access conditions that the +1 pillar determines. Scenarios diverge based on whether Vietnamese design firms are accumulating design complexity and IP depth at a rate that generates switching costs and commercial differentiation, or whether they remain in the design service model that generates revenue without building proprietary value. This driver is the primary differentiator between Scenario 1, where IP generation is not the strategic objective, and Scenario 3, where it is the central one.

The fourth variable driver is the pace of Vietnam's legal reclassification within the US export control framework and the associated progress toward trusted partner status more broadly. This driver operates as a gate function across multiple scenarios simultaneously: its value determines whether the VEU pathway is accessible for advanced packaging die inputs, whether full-featured EDA tools and commercial PDKs are available for chip design, and whether the bilateral equipment access relationships for wafer fabrication can be established within the project timeline. Unlike the other variable drivers, which are primarily shaped by domestic policy choices, this driver is co-determined by US interagency decisions that Vietnamese policy can influence but not control.

Vietnam's Positioning Options in the AI Semiconductor Value Chain

Scenario 0: FDI Host without Strategic Synchronization

Scenario 0 results in when all four variable drivers remain at low values: pillar desynchronization persists, compliance infrastructure develops slowly, IP generation remains limited to design services, and legal reclassification does not advance. This is the scenario that requires the least to go wrong, it is the natural outcome of inertia applied to the current starting position.

Vietnam continues to attract large-scale electronics and semiconductor FDI, but the four SET+1 pillars develop in isolation. ATP does not climb toward advanced packaging, design does not generate indigenous IP, fabrication lacks sufficient preconditions, and the geopolitical variable stalls at diplomatic positioning without translating into legal recognition. This is a scenario where FDI growth remains measurable but Vietnam's position in the value chain does not change in substance. Critically, this is also the highest-probability scenario absent coordinated policy intervention and serves as the baseline against which the value of the remaining scenarios should be assessed.

Scenario 1: ATP Hub

Scenario 1 results when the compliance and reclassification drivers remain at low to moderate values, but the existing FDI ecosystem continues to generate growth through scale expansion rather than technology ladder climbing. It does not require synchronization across SET+1 pillars beyond what the current FDI-driven dynamic already produces.

Vietnam consolidates and expands its presence in conventional assembly, testing, and packaging, leveraging the existing Intel and Amkor infrastructure to grow its global ATP market share from 1% toward the 8% target by 2032. The E pillar plays the leading role, with industrial clusters in Bac Ninh and Ho Chi Minh City reinforced as regional ATP centers. This is the lowest-risk pathway with the most established infrastructure base, but it does not alter Vietnam's qualitative position in the value chain and remains vulnerable to substitution by competing ATP centers in the region.

Scenario 2: Advanced Packaging Node

Scenario 2 results when the legal reclassification driver advances sufficiently to unlock VEU eligibility for advanced packaging inputs, and when the E pillar synchronizes with the +1 pillar to create the compliance environment that large-scale die imports require. It does not require high values on the IP generation driver, which is what makes it more tractable than Scenario 3 on a near-term timeline.

Building on the ATP foundation, Vietnam moves into advanced packaging, covering chiplet integration, 2.5D and 3D stacking, serving directly the AI chip production chain. This is the direction that Amkor's $1.6 billion investment in Bac Ninh is heading, and it represents the fastest-growing value segment within ATP in the post-Moore's Law era. This scenario requires the E and +1 pillars to operate in synchronization: an industrial ecosystem mature enough to support more complex processes, and a sufficiently credible legal standing to permit the importation of advanced dies as inputs for packaging.

Scenario 3: Chip Design Hub

Scenario 3 results when the compliance and reclassification drivers advance in combination with meaningful progress on the IP generation driver, specifically when EDA tool access improves sufficiently to support design complexity beyond the PMIC level and when architect-level engineering talent accumulates through some combination of domestic development and diaspora engagement.

Vietnam builds indigenous chip design capability with proprietary IP in segments including PMIC,

telecom ASICs, and IoT chips, generating value from chip architecture ownership rather than manufacturing services. FPT Semiconductor's export of power management chips to a Japanese distributor in late 2025 represents the first concrete signal that this scenario has a technical foundation to build on. This scenario demands the tightest synchronization between the S and T pillars: indigenous IP design capability cannot emerge without architect-level engineers and full-featured commercial EDA tool access. It is also the scenario most directly affected by US export controls on software and IP.

Scenario 4: Mature Node Foundry

Scenario 4 results in when all four variable drivers reach high values simultaneously, including the multi-jurisdiction compliance management capability that sustained fab operations require. It is the scenario with the most demanding combination of driver values and the longest timeline for those values to be achievable, which is why it is treated as a post-2030 objective in the realistic positioning analysis that follows.

Vietnam develops domestic wafer fabrication capability at the 28 to 32nm process node, serving domestic demand for telecom, defense, and IoT chips, with Viettel's Hoa Lac project as the first step toward pilot production by 2028. This is the scenario with the highest degree of strategic autonomy, creating real chip manufacturing capability on Vietnamese soil with value that extends beyond purely economic considerations. It is, however, the scenario requiring the longest time horizon, the largest capital commitment, and the most complex web of bilateral institutional relationships with equipment suppliers across the United States, Japan, the Netherlands, and South Korea.

These five scenarios form an evaluative matrix for the export control impact analysis in the following section. Scenario 0 serves as the no-intervention baseline. Scenario 1 is the least affected by export controls. Scenarios 2 and 3 face direct constraints at different technology layers. And Scenario 4 depends on the broadest and most complex set of equipment controls, making it the most sensitive to the overall trajectory of US-allied export control policy toward Vietnam.

II. The Impact of Export Control Mechanisms on Vietnam's Semiconductor Value Chain Development Capacity

Technology Control Map and Key Strategic Chokepoints

The Wassenaar Arrangement: The Multilateral Baseline

The Wassenaar Arrangement serves as the foundational international legal framework shaping Vietnam's ability to access core semiconductor and AI technologies. Unlike unilateral measures that can be adjusted by executive decision, Wassenaar regulations represent a consensus of more than 40 developed nations, including Vietnam's key technology partners such as Japan, South Korea, and the Netherlands, and therefore carry a durability and legitimacy that bilateral controls do not. For Vietnam, non-membership in the Wassenaar Arrangement creates an invisible but pervasive administrative barrier: every transaction involving chip design software, sensitive manufacturing equipment, or dual-use AI components must undergo end-user verification processes that member states impose on non-members as a matter of standard procedure, not political discretion.

The deepest impact of Wassenaar on Vietnam's semiconductor ambitions falls on dual-use AI technologies, systems capable of switching between civilian and military applications. Advanced image processing algorithms, high-performance DSP chips, and optical sensors used in autonomous systems all fall under strict Wassenaar control categories. For domestic chip design entities such as Viettel and FPT, this creates a technical bottleneck at the IP layer: they cannot easily import the most advanced IP libraries needed to develop specialized AI chips without demonstrating export control compliance standards that Vietnam's legal framework does not yet formally support. The consequence is not a hard block but a structural friction, technology transfers happen more slowly, at reduced functionality, and with higher transaction costs than for Wassenaar member states.

This compliance burden extends beyond chip design into the broader digital infrastructure stack. Operating AI training supercomputers requires high-speed data transmission protocols and physical-layer security algorithms that appear on Wassenaar dual-use control lists. The absence of a domestic legal framework equivalent to Wassenaar's standards

causes leading solution providers from the EU and Japan to offer only reduced-functionality commercial versions rather than complete technology packages, a limitation that affects not just individual enterprises but the capacity of Vietnam's AI data center ecosystem as a whole. For FDI enterprises operating in Vietnam, this translates into complex internal compliance management systems that raise the cost of deep supplier development with domestic firms, reinforcing the enclave dynamic discussed in the SET+1 analysis.

The long-term trajectory, however, is not fixed. Decree 259/2025/ND-CP represents Vietnam's first legislative step toward aligning domestic export control standards with international norms. If Vietnam can demonstrate credible and transparent dual-use goods management capabilities over time, the Wassenaar barrier has the potential to function as a technology passport rather than a gatekeeping mechanism, progressively unlocking access to EDA tools, IP libraries, and manufacturing equipment previously available only to formal member states. In parallel, Wassenaar pressure has already produced one unintended but strategically significant effect: it has accelerated Vietnamese interest in the RISC-V open instruction set architecture, which sits largely outside traditional export control frameworks and offers a path to indigenous chip development that is structurally less exposed to multilateral licensing friction.

US Export Controls: Unilateral Escalation on Top of the Multilateral Baseline

If Wassenaar establishes the floor of the control architecture, US Bureau of Industry and Security regulations represent the ceiling, a layer of unilateral controls that operates on top of the multilateral framework and moves significantly faster in response to geopolitical developments. For Vietnam, BIS regulations have created technology red zones across all three segments of the domestic semiconductor ecosystem through three principal control groups, each operating at a different point in the value chain.

The first and most structurally decisive group concerns advanced semiconductor manufacturing equipment. EUV lithography systems and atomic layer deposition equipment remains the exclusive domain of a handful of corporations, ASML in the Netherlands and Applied Materials in the United States, whose export behavior is now directly governed by BIS controls extended through the Foreign Direct Product Rule. The tightening of controls on equipment used for sub-14nm processes has created a market entry barrier that is effectively insurmountable for Vietnam's midstream fabrication ambitions in the near term.

The second control group centers on high-performance AI components, specifically GPUs and AI accelerators exceeding BIS performance thresholds. Vietnam currently sits in what the AI Diffusion Rule framework classified as Tier 2, not prohibited from receiving advanced chips but subject to quantity limits, end-user verification requirements, and VEU certification processes for large-scale deployments. The practical consequence is a performance ceiling on Vietnam's AI data center infrastructure: accessing H100, H200, or Blackwell-tier chips at scale requires demonstrating compliance infrastructure that Vietnam is still building. This creates a compounding disadvantage, where countries that face no such restrictions can build AI infrastructure faster and at lower compliance cost, widening the computational gap over time regardless of Vietnam's investment intentions.

The third control group operates at the materials layer, where BIS requirements intersect with supply chain realities in ways that directly threaten Vietnam's existing ATP strength. CHIPS Act 2.0 compliance requirements compel enterprises operating in Vietnam to demonstrate that raw material sourcing is free from dependence on sanctioned Chinese entities, a requirement that is technically straightforward in principle but commercially painful in practice, given that alternative sourcing from Japan or Australia carries a 25 to 40%price premium over Chinese suppliers. For packaging operations where margins already sit at 5 to 8 percent, this cost differential is not merely a compliance burden but an existential arithmetic problem.

EU Dual-Use Controls: A Partial Buffer Zone

Unlike the USUS approach, which uses the Entity List as a flexible punitive instrument and applies extraterritorial reach through the Foreign Direct Product Rule, the European Union's control mechanism under Regulation 2021/821 operates on a more predictable multilateral legal foundation. The EU classifies dual-use goods based on specific

technical criteria rather than shifting end-user assessments, which allows Vietnamese enterprises cooperating with European technology partners to follow a more stable compliance roadmap. This difference in regulatory philosophy creates a meaningful buffer zone: equipment such as DUV lithography systems and precision measurement tools from European suppliers can in some cases be accessed without facing the same political friction as equivalent US-origin goods.

The EU's concept of strategic autonomy, focused on protecting economic value rather than weaponizing supply disruptions, also means that diversifying toward European supply sources provides Vietnam with a degree of hedging against sudden US policy shifts. By integrating design tools from Siemens EDA or equipment from European precision machinery suppliers, Vietnamese enterprises reduce their exposure to any single jurisdiction's executive decisions.

However, the EU buffer zone has important limits that must not be overstated. The most significant is the divergence between EU-level policy and member state implementation: in the case of ASML, the Dutch government has applied independent restrictions on EUV lithography exports that go beyond EU-level consensus. This means that supply chain diversification toward Europe requires navigating member state laws individually, Germany for precision machinery, the Netherlands for lithography, France for certain software, rather than dealing with a single policy framework. Furthermore, European machinery frequently incorporates US intellectual property, meaning that the Foreign Direct Product Rule can reach European-origin goods when their US-content threshold is exceeded. True supply chain diversification toward the EU therefore requires component-level origin mapping, not simply supplier geography switching.

China's Export Controls on Strategic Materials: Pressure from the Opposite Direction

While the United States and its Western allies focus on controlling the "top end" of the value chain, namely design and manufacturing equipment, China has countered by tightening its grip on the "base end," that is, raw materials and basic chemicals. China's imposition of export controls on gallium and germanium from late 2023, followed by graphite and rare earth elements during 2024 and 2025, directly targeted the greatest vulnerability of global semiconductor manufacturers: their dependence on cheap and stable raw material supplies. For Vietnam, a country positioning itself as a leading ATP hub, these risks have become direct variables threatening the profit margins and production schedules of major technology complexes.

The greatest impact of China's control strategy on Vietnam's ecosystem lies in the vulnerability of the Downstream segment. Packaging facilities in Vietnam, whether owned by American or South Korean corporations, continue to import large volumes of specialty chemicals and substrate materials from China.[15] According to 2025 trade data, China still controls up to 94% of global gallium output and 83% of global germanium output, elements that are essential for producing compound semiconductors used in fast charging, 5G devices, and radar systems. China's requirement for special export licenses has extended customs clearance times from three weeks to between eight and twelve weeks, directly increasing warehousing costs and supply disruption risks for enterprises.

China's retaliation has also created a dual pressure on compliance costs. To meet requirements from the US side, such as those introduced by the CHIPS Act 2.0 enacted in 2025, enterprises in Vietnam are compelled to demonstrate that their raw material sources are free from dependence on sanctioned Chinese entities. However, sourcing alternative supplies from Japan or Australia typically comes with prices that are 25% to 40% higher. Data analysis indicates that for the memory chips and general-purpose logic chips that Vietnam is currently packaging, profit margins are already thin, at only around 5% to 8%. A sharp rise in material costs could turn FDI projects in Vietnam from profitable to loss-making if there are no compensating mechanisms such as tariff offsets or government infrastructure subsidies.

In addition, China's controls targeting rare earth elements are directly threatening Vietnam's ambitions to expand into AI device and electric vehicle (EV) manufacturing. While some previous, older reports had placed Vietnam's reserves as high as 22 million tons, the US Geological Survey Mineral

[15] This statement is based on information gathered through conversations with industry representatives.

Commodity Summaries 2025 report, released in March 2025, significantly revised this estimate downward to 3.5 million tons. Regardless of the precise reserve figure, current extraction capacity meets less than 1% of domestic demand. China's ban on exporting rare earth separation and refining technology in late 2023 has created an enormous technical barrier. Vietnam must still send raw ore to China for refining before importing it back in the form of permanent magnets or high-power semiconductor components, leaving the domestic AI value chain effectively locked into Beijing's processing capacity.

A particularly alarming dimension is the emergence of reciprocal blacklists. Under new regulations from China's State Council in early 2026,[16] enterprises in third countries such as Vietnam that enforce US restrictions too strictly, causing harm to Chinese businesses, may face immediate cuts to strategic material supplies.[17] This places companies such as Samsung and Intel in Vietnam in a dilemma: comply with US law to retain technology licenses, while simultaneously facing the risk of China cutting off their material lifelines. The intersection of these two control systems turns Vietnam into a risk buffer zone, where any misstep in dual-use goods management policy can lead to serious economic consequences.

China's controls are compelling the Vietnamese Government to restructure its national materials strategy. Data from the Ministry of Industry and Trade shows that the shift toward mineral alliances with Australia and Canada is accelerating, but the construction of domestic refining facilities is not expected to reach industrial-scale operation until 2028. In the short-term scenario through to the end of 2026, Vietnam still faces the risk of localized supply disruptions.

Implications for Vietnam's Strategic Scenarios in the AI Semiconductor Value Chain

Before proceeding to the scenario-by-scenario analysis, it is necessary to establish clearly the scope and analytical perspective of this section. The analysis below approaches export control measures as a discrete policy variable, examining specifically how existing control mechanisms operate, which technology layers are constrained and by whom, and how each of Vietnam's strategic scenarios is affected in technical and legal terms. This perspective is intentionally bounded: it is not a comprehensive assessment of Vietnam's foreign relations, nor does it imply that Vietnam's capacity to develop its semiconductor value chain depends entirely on any single bilateral relationship.

In practice, the export control architecture that Vietnam is navigating is multi-layered and multi-actor. It encompasses the US Bureau of Industry and Security under the Export Administration Regulations, the Wassenaar Arrangement with more than forty member states, the EU's dual-use control framework under Regulation 2021/821, and China's strategic material controls covering gallium, germanium, graphite, and rare earth processing technology. Each layer operates under its own logic, covers a distinct scope of goods and technologies, and exerts different pressures on different segments of the value chain. The scenario analysis below attempts to distinguish clearly which control layer is acting on which scenario, rather than collapsing all constraints into a single generalized claim about "Western barriers."

The five scenarios, as mentioned above, are not mutually exclusive, and the impact of export controls on each is not static. These controls continue to evolve as the policy positions of relevant actors adjust, as illustrated by the shifts between the Biden-era AI Diffusion Rule, the Trump administration's subsequent modifications, and the ongoing regulatory uncertainty that leaves industry in an interim phase as of early 2026. Vietnam's own legal standing within these control frameworks is similarly in flux, with Decree 259/2025/ND-CP representing a first step toward international alignment that has not yet been tested against the full requirements of partner country compliance expectations. The

[16] Including the State Council Decree No. 834, Provisions of the State Council on the Security of Industrial and Supply Chains and the State Council Decree No. 835, Regulations of the People's Republic of China on Countering Unjustifiable Extraterritorial Jurisdiction Measures Imposed by Foreign States.

[17] De, R., Hickey, A. S., Kendler, T., Kennedy, G., Shie, G., Wong, J. K. C., Zhang, J., Diament, H. G., Keeler, T. J., Soliman, T. A., & Liu, R. (2026). *China Expands Its Playbook: New Industrial Supply Chain and Counter-Extraterritoriality Regulations Create Direct Compliance Conflicts for Multinationals.* Mayer Brown. https://www.mayerbrown.com/en/insights/publications/2026/05/china-expands-its-playbook-new-industrial-supply-chain-and-counter-extraterritoriality-regulations-create-direct-compliance-conflicts-for-multinationals.

purpose of this analysis is therefore not to render a verdict on which scenarios are viable or foreclosed, but to identify precisely where the legal and technological chokepoints lie, and where Vietnamese policy has genuine leverage to act.

Scenario 0: FDI Host without Strategic Synchronization

Scenario 0 is the only scenario in this analysis where export controls do not function primarily as a barrier to ambition. This is the scenario of continued FDI attraction without strategic synchronization across the SET+1 pillars, and its relationship with the export control architecture is therefore paradoxical: the current control environment does not cause Scenario 0, but it actively sustains it by making the path of least resistance, expanding existing ATP operations without attempting to climb the technology ladder, also the path of lowest regulatory friction.

The mechanism operates through three reinforcing channels. The first is what might be called regulatory gravity toward the permitted tier. Vietnam's current Tier 2 classification under US chip export frameworks, combined with its non-membership in the Wassenaar Arrangement, creates a technology access environment where the activities that are easiest to pursue are precisely the activities that generate the least value: conventional packaging, standard testing, and assembly operations that sit well below the thresholds of any of the four control regimes examined above. An enterprise expanding conventional ATP capacity in Bac Ninh or Ho Chi Minh City faces minimal regulatory friction, no EDA tool restrictions, no PDK access barriers, no AI chip import licensing requirements, no equipment controls of consequence. The regulatory environment is, in effect, permissive toward the lower-value segments and restrictive toward the higher-value ones. In the absence of deliberate policy intervention to overcome this gradient, enterprises will rationally concentrate activity where regulatory friction is lowest, which is precisely the zone that generates the least value for Vietnam's domestic ecosystem.

The second channel operates through compliance cost allocation within MNC decision-making. When a multinational corporation such as Intel, Samsung, or Amkor evaluates how deeply to integrate domestic Vietnamese suppliers into its operations, the Wassenaar non-membership status of those suppliers creates a quantifiable compliance overhead: every transaction involving sensitive components or processes requires additional end-user verification, documentation, and internal approval workflows that add cost and delay without adding technical value. The rational response, from the perspective of MNC procurement, is to source sensitive inputs from established suppliers in Wassenaar member states and limit domestic Vietnamese supplier engagement to non-controlled consumables and low-sensitivity subassemblies. This is not a deliberate exclusion of Vietnamese firms; it is a compliance cost optimization that produces exclusion as a byproduct. The result is the enclave economy structure identified in the SET+1 analysis: large, sophisticated FDI operations coexisting with a domestic supplier base that remains structurally locked out of the technology-intensive portions of the value chain. Scenario 0 is, in this sense, the equilibrium that the export control architecture naturally produces when no countervailing policy force is applied.

The third channel is the suppression of domestic enterprise risk appetite. For Vietnamese firms such as FPT, Viettel, and CMC that do have the technical ambition to move into higher-value segments, the export control environment introduces a specific category of risk that does not exist for their counterparts in Wassenaar member states: legal uncertainty around technology acquisition. Accessing full-featured EDA tools, commercial PDKs, or advanced IP cores require navigating end-user verification processes whose outcomes are not guaranteed and whose timelines are unpredictable. This uncertainty has a well-documented effect on enterprise investment behavior: it shifts capital allocation away from technology-intensive activities with uncertain regulatory approval timelines toward lower-risk activities with more predictable cost structures. At the aggregate level, the sum of these individual enterprise decisions produces a domestic technology sector that is systematically underinvested in the capabilities that would be necessary to escape Scenario 0, not because the technical ambition is absent, but because the regulatory risk premium attached to pursuing it is high enough to suppress the investment.

What makes Scenario 0 particularly difficult to escape through incremental policy adjustment is that these three channels are mutually reinforcing. Regulatory gravity toward the permitted tier reduces the domestic supplier base's exposure to technology-intensive processes, which in turn limits the track record and compliance credibility that would be

necessary to reduce verification overhead, which in turn sustains the compliance cost allocation decisions that keep MNCs from developing domestic suppliers more deeply, which in turn suppresses domestic enterprise risk appetite for technology-intensive investment. The loop closes on itself, and each iteration reinforces the conditions for the next.

The implication for Vietnam's export control policy is therefore not simply that specific technology restrictions need to be lifted though that matters but that the structural gradient itself needs to be reversed. As long as the regulatory environment makes lower-value positions in the supply chain appear easier to occupy and expand at scale, Scenario 0 will remain the gravitational attractor of the system regardless of investment volumes, FDI headline numbers, or policy ambition. The conditions for escaping Scenario 0 are therefore not primarily technical but institutional: they require Vietnam to reduce the regulatory risk premium attached to technology-intensive activities through credible export control legal infrastructure. This is the gap that policymakers believe Decree 259/2025/ND-CP begins to address, even as the distance between a first legislative step and a fully credible compliance framework remains to be demonstrated in practice.

Scenario 1: ATP Hub

Of the five scenarios, ATP hub consolidation has the most straightforward relationship with the export control architecture: it is the scenario least directly constrained by the technology-intensive control categories, yet it is simultaneously the scenario most materially threatened by the controls that operate at the input layer rather than the output layer. The distinction matters because the risks facing Scenario 1 are not primarily about what Vietnam cannot access — they are about the stability and cost structure of what it already has.

Conventional assembly, testing, and packaging operations sit comfortably within the technology tiers that all four control regimes examined above treat as relatively uncontroversial. Standard wire bonding, flip-chip interconnect, wafer-level packaging for mature-node devices, and associated testing equipment do not trigger the high-performance thresholds of BIS AI chip controls, do not require the advanced manufacturing equipment licenses that bind Scenario 4, and do not demand the EDA tool access or PDK relationships that constrain Scenario 3. In this sense, Vietnam's existing ATP infrastructure, anchored by Intel processing half of its global packaging and test volume in Ho Chi Minh City, Amkor targeting 3.6 billion units annually from Bac Ninh, and Hana Micron and Onsemi contributing additional OSAT capacity, operates in a regulatory space that is genuinely accessible under current export control conditions. This is Scenario 1's structural advantage: it does not require Vietnam to resolve any of the hard legal questions around Wassenaar membership, Tier 1 reclassification, or EDA tool licensing that the higher-value scenarios depend on.

However, the most direct export control threat to Scenario 1 does not come from Washington but from Beijing. China's controls on gallium, germanium, specialty chemicals, and substrate materials strike at the material input base that Vietnam's ATP operations depend on for continuous production. The arithmetic of this threat is precise and uncomfortable. With profit margins on conventional packaging already sitting at 5 to 8 percent, and with alternative sourcing from Japan or Australia carrying a 25 to 40%price premium over Chinese suppliers, even a partial and sustained shift in material sourcing is sufficient to compress margins to levels that make FDI-anchored packaging operations commercially marginal without government compensating mechanisms.

The compliance dimension compounds this pressure. CHIPS Act 2.0 requirements compel enterprises operating in Vietnam to demonstrate that raw material sourcing is free from dependence on sanctioned Chinese entities, a requirement that is not merely a paper certification but demands actual supply chain restructuring that takes time, capital, and relationships that do not yet exist at the necessary scale. An enterprise simultaneously facing Chinese retaliatory supply cuts and US compliance requirements to move away from Chinese suppliers is caught in a squeeze that no amount of production efficiency can fully absorb. For Scenario 1 specifically, where the value proposition rests on reliable, high-volume, cost-competitive packaging operations, supply chain instability of this kind is not a manageable risk, it is a structural threat to the business model itself.

Vietnam's Ministry of Industry and Trade data indicates that the shift toward mineral alliances with Australia and Canada is accelerating, but domestic

refining capacity is not expected to reach industrial-scale operation until 2028. This creates a window of material vulnerability through at least the end of 2026 during which Scenario 1 remains exposed to localized supply disruptions that neither the Vietnamese government nor the FDI enterprises operating in Vietnam have fully buffered against.

The MOFCOM reciprocal blacklist regulations introduced in early 2026 add a further dimension of risk that is specific to Vietnam's position as a country hosting both US-aligned semiconductor MNCs and significant Chinese material supply relationships. Enterprises such as Samsung, Intel, and Amkor are legally required to comply with US export control and supply chain provenance requirements but doing so in ways that visibly harm Chinese business interests now carries the risk of triggering retaliatory cuts to the very material supplies that their Vietnam operations depend on. This is not a hypothetical tension: it is a structural dilemma embedded in the operating environment of every major ATP facility in Vietnam.

For Scenario 1, this dilemma has a specific operational implication. The more rigorously Vietnam enforces US compliance requirements, a prerequisite for building the trust signal necessary to eventually move toward higher-value scenarios, the more it exposes its existing ATP operations to Chinese material retaliation. Conversely, the more Vietnam accommodates Chinese material relationships to protect ATP margins, the more it risks the compliance standing with US partners that its longer-term strategic positioning depends on. This is not a dilemma that Scenario 1 alone creates, but it is the scenario in which the dilemma is felt most acutely in the near term, because the economic consequences of getting it wrong land directly on the operations that currently constitute Vietnam's greatest semiconductor strength.

An underappreciated constraint on Scenario 1 concerns the boundary between conventional and advanced packaging. As Amkor's Bac Ninh facility scales toward its target output profile and begins targeting higher-value packaging formats, such as chiplet integration, 2.5D and 3D stacking, it will progressively encounter the die input restrictions that define the threshold between Scenario 1 and Scenario 2. Packaging advanced AI accelerator dies, or high-bandwidth memory stacks require importing those dies as inputs, and those inputs are subject to the same BIS controls that govern finished AI chip exports to Tier 2 destinations. The moment Scenario 1 reaches for its highest-value adjacent opportunity, it runs into the export control boundary that separates it from Scenario 2 and crossing that boundary requires the legal and institutional progress that Scenario 1 alone cannot generate. This boundary is the active constraint on how much value Vietnam can extract from the Amkor investment that is already in the ground. Resolving it is therefore the condition that determines whether Vietnam's ATP hub becomes a platform for value chain ascent or a ceiling that contains it.

Scenario 2: Advanced Packaging Node

Advanced packaging, covering chiplet integration, 2.5D interposer-based integration, and 3D stacking, is simply not a more sophisticated version of conventional ATP. It is a fundamentally different value proposition: rather than packaging a single chip into protective housing, it integrates multiple specialized dies into a unified high-performance system that achieves computational density impossible at the single-die level. This architectural shift is what makes advanced packaging the fastest-growing segment of the semiconductor value chain in the post-Moore's Law era, and it is what makes Amkor's $1.6 billion commitment to Bac Ninh strategically significant beyond its scale alone. The facility is not being built to do more of what Intel already does in Ho Chi Minh City. It is being built to serve a different and higher-value market: the integration of AI accelerator chiplets, high-bandwidth memory stacks, and logic dies into the complex multi-chip modules that data center AI infrastructure demands.

The export control implication follows directly from this technical reality. Advanced packaging is an integration service, and its value is proportional to the sophistication of the dies being integrated. A 2.5D packaging facility that can only integrate mature-node dies produces a fundamentally different and lower-value output than one that can integrate sub-7nm AI accelerator dies with HBM memory stacks. The export control architecture therefore does not constrain advanced packaging at the equipment or process level. It constrains it at the input level, by determining which dies can legally enter Vietnam as packaging feedstock.

Vietnam's current Tier 2 classification under US chip export frameworks means that advanced AI accelerator dies, the highest-value inputs for the advanced packaging market, are subject to the same BIS performance threshold controls as finished AI chips. An HBM memory stack, an AI accelerator die from TSMC's N3 or N4 process, or a high-performance logic chiplet from a leading foundry are not freely importable into Vietnam as packaging inputs simply because they are unfinished components rather than finished products. The end-use and end-user verification requirements that govern advanced chip exports apply to the dies themselves, meaning that Amkor's Bac Ninh facility must navigate BIS licensing requirements for its highest-value input materials in the same way that a Vietnamese data center operator must navigate them for finished GPU imports.

This creates a precise and commercially significant limitation. A facility can be equipped with the full process capability for advanced packaging, covering TSV drilling, hybrid bonding, and high-density substrate integration, without those capabilities being fully monetizable if the die inputs that would generate the highest margins cannot be imported at scale under current export control conditions. The capital investment is in the ground; the regulatory condition that determines its return on investment is not yet resolved. This is the defining characteristic of Scenario 2's relationship with the export control architecture: it is not a scenario that is blocked from starting, but one where the ceiling on value capture is set by a legal classification rather than a technical or commercial limitation.

The Validated End User certification program offers a potential resolution to this chokepoint. It provides a general authorization for US exports of advanced chips and components to pre-approved facilities in Tier 2 countries, operating under a presumption of license approval for qualifying transactions. VEU certification would in principle unlock the ability to import advanced dies at the scale necessary to serve the AI chip packaging market without individual transaction licensing. The pathway exists and is designed for exactly this kind of large-scale, high-compliance industrial deployment.

However, VEU certification is not a bureaucratic formality. It requires demonstrating compliance infrastructure covering physical security measures, cybersecurity standards, personnel vetting, and end-use monitoring systems that meet BIS specifications, and it requires Vietnam as a host country to provide a regulatory environment that supports rather than complicates those compliance obligations. This is where Vietnam's non-Wassenaar status and the early-stage development of its domestic export control legal framework become directly relevant to Scenario 2's commercial viability: VEU applications for facilities operating in countries with underdeveloped dual-use goods management frameworks face higher scrutiny and less predictable approval timelines than equivalent applications from facilities in countries with established compliance track records. The regulatory risk premium identified in Scenario 0 does not disappear in Scenario 2. It concentrates on the VEU certification bottleneck.

Scenario 2's viability at its highest-value tier depends more on the +1 pillar: Vietnam's legal standing in the US export control framework. The binding constraint is whether Vietnam can achieve the legal reclassification, including removal from strategic export control lists, progress toward trusted partner status, and credible Wassenaar-aligned domestic compliance infrastructure, that would allow the die input restrictions to be resolved at the facility level through VEU or equivalent authorization mechanisms. This makes the +1 pillar not a supporting element of Scenario 2 but its rate-limiting step.

A final consideration specific to Scenario 2 concerns the competitive dynamics of advanced packaging in Southeast Asia. Malaysia, through its Penang semiconductor cluster, and Singapore, through its established trusted partner status with US export control authorities, are both actively competing for the advanced packaging investment that Vietnam is seeking to attract and retain. Both operate from a more favorable regulatory baseline: Malaysia's longer track record in OSAT operations has generated deeper compliance infrastructure, and Singapore's standing with multiple export control regimes means that die input restrictions of the kind constraining advanced packaging facilities in Vietnam do not apply with the same intensity elsewhere in the region. Vietnam's window to establish itself as the leading advanced packaging node in Southeast Asia is therefore not indefinitely open. It is a function of how quickly it can resolve the legal and institutional conditions that currently constrain Scenario 2's value ceiling relative to

regional alternatives that are already operating without those constraints.

Scenario 3: Chip Design Hub

Scenario 3 is defined by a cluster of interlocking constraints that operate simultaneously across the software, IP, and legal recognition layers of the technology stack. The chip design process can be understood as a sequence of technology dependencies, each of which must be resolved before the next becomes relevant. A design engineer begins with an architectural concept, translates it into RTL code, simulates and verifies its functional behavior, maps it to a physical layout optimized for a specific manufacturing process, runs timing and power sign-off against that process's constraints, and finally submits a tape-out package to a foundry for fabrication. Each stage in this sequence depends on tools, IP libraries, and process data that sit within the export control perimeter in ways that are specific and consequential.

At the architectural stage, the choice of processor core, ARM, RISC-V commercial implementations, or proprietary architectures, determines the IP licensing relationships that the design depends on. ARM architecture licenses for high-performance cores carry end-use verification requirements under both Wassenaar and BIS frameworks that are more burdensome for entities in non-member states. Commercial RISC-V implementations from vendors such as SiFive carry similar, though somewhat lighter, licensing friction. The consequence is that Vietnamese design firms building on licensed processor IP face a higher transaction cost and longer approval timeline than counterparts in Wassenaar member states for accessing the same architectural foundations.

At the simulation and verification stage, full-featured EDA tool suites from Synopsys and Cadence are the industry standard, and there is no commercially viable alternative for production-grade chip design. These tools appear on Wassenaar dual-use control lists and are subject to BIS export licensing requirements for certain advanced modules, particularly those relevant to mixed-signal design, RF front-end development, and high-performance digital synthesis. The versions currently accessible in Vietnam are not uniformly restricted, but the most advanced modules, those needed for designing chips at the complexity level required to generate meaningful IP differentiation, face end-user verification requirements that Vietnam's current legal framework does not fully satisfy. As HUST's experience demonstrates, this is not a theoretical constraint: it manifests in practice as an inability to access commercial PDKs and the consequent reliance on open-source process platforms that do not correspond to any foundry's actual production process node.

At the physical implementation and tape-out stage, the dependency on foundry PDKs is absolute. A PDK is not merely a technical library, it is a legal and commercial relationship between a design house and a foundry that includes confidentiality obligations, end-use commitments, and export control compliance certifications that the foundry must satisfy with respect to its home country's regulatory requirements. TSMC, operating under Taiwan's export control framework and subject to US Foreign Direct Product Rule provisions, applies its own end-user screening to PDK licensing decisions. A Vietnamese design firm seeking a commercial PDK from TSMC for a 28nm or 40nm process is not simply making a technical procurement decision, it is entering a compliance relationship that TSMC must approve within the constraints of the regulatory environment governing its own operations.

A design firm that cannot access full-featured EDA tool modules produces designs of lower complexity. Lower-complexity designs generate less defensible IP. Less defensible IP attracts fewer anchor customers willing to commit to long-term supply relationships. Fewer anchor customer commitments reduce the revenue base available to invest in the next generation of design capability. And a thinner revenue base makes it harder to absorb the compliance costs and approval timelines associated with accessing better tools and process relationships in the next design cycle. The export control constraints do not simply limit what Vietnamese design firms can do today, they limit the rate at which those firms can accumulate the capabilities, track record, and commercial relationships that would allow them to access better technology tomorrow.

This compounding dynamic is what makes the gap between open-source design platforms and commercial EDA tool access so strategically significant. It is not merely a question of tool quality in any given design cycle. It is a question of whether Vietnamese design firms are accumulating capability

at a rate that allows them to close the gap with design houses in more favorable regulatory environments, or whether the export control constraints are holding the rate of capability accumulation below the threshold necessary for the gap to close at all.

The pressure that Wassenaar and BIS controls place on licensed IP access has accelerated Vietnamese interest in the RISC-V open instruction set architecture, which sits largely outside the traditional export control perimeter. FPT Semiconductor's PMIC exports to Japan and Viettel's telecommunications chip development have both drawn on open-architecture approaches that reduce dependence on controlled IP licensing relationships. This is a genuine strategic opening: designs built on RISC-V cores and verified on open-source EDA platforms such as OpenROAD can be developed with significantly lower regulatory friction than equivalent designs built on ARM or commercial RISC-V implementations with commercial EDA tool chains.

However, the RISC-V opening has structural limits that become binding precisely at the point where Scenario 3 needs to generate the most value. Open-source EDA tools and process platforms are adequate for relatively simple designs, PMICs, basic microcontrollers, straightforward digital logic, but they fall short of the verification coverage, timing accuracy, and physical implementation quality required for more complex designs such as multi-core AI accelerators, high-speed interface chips, or mixed-signal designs with stringent analog specifications. The market segments where RISC-V and open-source EDA tools are sufficient are also the segments with the lowest IP differentiation potential and the highest exposure to commodity competition. Scenario 3's ambition to establish Vietnam as a chip design hub with proprietary IP requires eventually moving beyond what open-architecture platforms can support, and that move requires resolving the EDA tool access and PDK relationship constraints that the export control architecture currently imposes.

FPT Semiconductor's export of power management chips to a Japanese distributor in late 2025 under a multi-year contract is the most concrete evidence available that Scenario 3 has a technical foundation to build on. The chips in question are PMICs designed to meet Japanese industrial reliability standards, which are among the most stringent in the global electronics industry. This achievement demonstrates that Vietnamese design firms can produce commercially viable IP that satisfies demanding international quality requirements, a proof of concept that matters for the scenario's credibility.

What it also reveals, however, is the current ceiling. PMICs are relatively simple analog and mixed-signal designs that can be developed on mature process nodes with moderate EDA tool requirements. They represent the segment of chip design that is most accessible within the current export control constraints, and they are the segment with the lowest IP differentiation potential relative to the complexity of design that a genuine chip design hub would need to produce. The FPT achievement is a necessary first step, but the distance between a successful PMIC export and a design hub capable of producing AI accelerator IP, high-speed SerDes chiplets, or advanced RF front-end designs is the distance that the export control architecture currently makes most difficult to traverse.

Vietnam's legal standing within the export control frameworks that govern EDA tool access, PDK licensing, and IP core availability. The prospect of Vietnam's removal from US strategic export control lists, if realized, would unlock access to full-featured EDA tool suites and commercial PDK relationships that are currently unavailable or available only in restricted form. This single legal reclassification would have a more immediate and direct impact on Scenario 3's viability than any amount of additional investment in university programs, laboratory equipment, or design center infrastructure, because it would resolve the compounding constraint at its source rather than attempting to work around it at each individual stage of the design cycle.

Decree 259/2025/ND-CP represents the first domestic legal step toward the compliance framework that would support this reclassification. But the distance between a first legislative step and the demonstrated track record of dual-use goods management that Wassenaar member states and BIS require before extending full technology access remains substantial, and it is a distance that cannot be shortened by policy declaration alone. It requires years of consistent enforcement, transparent reporting, and verifiable end-use monitoring that build the institutional credibility that legal reclassification ultimately rests on.

Scenario 4: Mature Node Foundry

Building a wafer fabrication facility capable of producing chips at the 28 to 32nm node requires a specific and largely non-substitutable set of equipment categories, each of which carries its own export control profile. The lithography layer is the most discussed but not the most immediate binding constraint. EUV lithography, which is required for process nodes below approximately 7nm, is effectively inaccessible to Vietnam under current conditions, but this is not relevant to the 28 to 32nm target, which can be achieved with deep ultraviolet lithography systems. DUV systems from ASML are subject to Dutch government export controls that have tightened progressively since 2023, but they are not categorically prohibited for a 28nm application in the way that EUV systems are. The relevant question for Scenario 4 is therefore not whether Vietnam can access EUV, it cannot and does not need to, but whether it can sustain reliable access to DUV systems and the associated immersion lithography consumables over the multi-year equipment procurement and facility ramp timeline that a fab construction project requires.

Beyond lithography, the equipment dependency map extends across deposition systems covering CVD, ALD, and PVD from Applied Materials and Lam Research, etch systems for both dielectric and metal layers, ion implantation equipment, chemical mechanical planarization tools, and the metrology and inspection systems from KLA and Applied Materials that are necessary for process control and yield management. Each of these equipment categories involves US-origin technology, and each is therefore subject to BIS Export Administration Regulations in ways that require end-use certification and, in some cases, license applications. The Foreign Direct Product Rule further extends US jurisdiction to equipment from non-US suppliers that incorporates US-origin components or manufacturing technology above applicable thresholds, which in practice means that a significant portion of the Japanese and Korean equipment that a 28nm fab would also require carries indirect US regulatory exposure.

What distinguishes Scenario 4's export control challenge from those of the other scenarios is not the severity of any individual constraint but the number of jurisdictions that must be navigated concurrently. A chip design hub needs to resolve its EDA tool and PDK access primarily within the US and Wassenaar frameworks. An advanced packaging facility needs to resolve its die input restrictions primarily within the US Tier 2 classification system. A mature node foundry needs to maintain active, compliant procurement relationships with equipment suppliers across the United States, Japan, the Netherlands, and South Korea simultaneously, each of which applies its own export control screening to each transaction, and any one of which can independently create a gap in the equipment supply chain that halts or delays the fab construction timeline.

This simultaneity problem is compounded by the fact that semiconductor manufacturing equipment procurement is not a one-time transaction. A fab requires ongoing equipment upgrades, spare parts, process consumables, and technical support relationships that involve continuous cross-border technology flows over the operational lifetime of the facility. A compliance failure or diplomatic friction with any one supplier's jurisdiction does not simply delay procurement. It can interrupt production at a running facility in ways that generate losses measured in hundreds of millions of dollars per day. The institutional relationships that Scenario 4 require are therefore not relationships that can be established once and maintained passively. They require continuous investment in compliance infrastructure, diplomatic engagement, and bilateral trust-building that places demand on Vietnamese institutional capacity well beyond what any of the other scenarios require.

The Dutch government's independent application of export restrictions on ASML equipment beyond EU-level policy has created a specific and practically significant constraint for Scenario 4. While DUV systems are not subject to the same categorical prohibition as EUV systems, the progressive tightening of Dutch export licensing for lithography equipment to non-allied destinations means that procurement of the immersion DUV systems needed for 28nm production requires navigating a bilateral licensing process with the Dutch government that is separate from, and in some respects more unpredictable than, the US BIS licensing process. For a fab construction project with a target pilot production date of 2028, the timeline implications of extended Dutch export licensing review are not abstract. They map directly onto construction schedules, equipment installation sequences, and the pilot production milestones that the project's financing and political commitments depend on.

This is the practical meaning of the multi-jurisdiction simultaneity problem for Scenario 4: the critical path of the Hoa Lac project runs not only through Vietnamese government approvals and Viettel's capital mobilization but through export licensing decisions in Washington, the Hague, Tokyo, and Seoul that are made on timelines and under criteria that Vietnamese policymakers cannot fully control or predict.

Scenario 4 also faces the material dependency problem identified in Scenario 1, but in a more acute form. A running semiconductor fabrication facility consumes large volumes of specialty process gases, ultra-high-purity chemicals, photoresist, and CMP slurry on a continuous basis. Many of the upstream precursor materials for these process chemicals involve Chinese supply chains, and China's export controls on strategic materials create a supply reliability risk that is more operationally consequential for a fab than for a packaging facility. A packaging facility that faces a specialty chemical supply disruption can in many cases substitute materials or adjust production scheduling without stopping the line. A wafer fab operating in a tightly controlled process environment has much less flexibility. Process chemical substitutions require extensive requalification that takes months, and production interruptions at the wafer level generate losses that cascade through the entire manufacturing pipeline.

The reciprocal blacklist dynamic introduced by MOFCOM regulations in early 2026 is therefore particularly significant for Scenario 4. A domestic fab that sources its equipment from US-aligned suppliers while simultaneously depending on Chinese precursor material supply chains sits at the exact intersection of the two competing control systems. Any diplomatic escalation that triggers either US technology access restrictions or Chinese material supply cuts lands on a facility whose operational continuity depends on both simultaneously.

Scenario 4 carries the highest degree of strategic autonomy among the five scenarios precisely because domestic wafer fabrication capability creates a chip supply that is not dependent on foreign foundry access, foreign packaging services, or foreign design tool licensing in the same way that the other scenarios are. For applications in telecommunications infrastructure, defense electronics, and government IoT systems, the ability to produce chips on Vietnamese soil under Vietnamese operational control has a strategic value that extends well beyond its economic return on investment. This is why Scenario 4 is a national priority rather than purely a commercial decision.

However, the preconditions for achieving that strategic autonomy are themselves deeply dependent on the international relationships and export control standing that the scenario is ultimately designed to reduce dependence on. Vietnam cannot build a domestically autonomous chip manufacturing capability without first successfully navigating the multi-jurisdiction equipment procurement relationships, bilateral compliance frameworks, and material supply diversification strategies that the export control architecture requires. The path to strategic autonomy runs through, not around, the international technology access system. This creates a sequencing imperative that is often underappreciated in policy discussions about Scenario 4: the institutional investments in export control legal infrastructure, bilateral compliance relationships, and material supply diversification that enable equipment procurement are not preparatory steps that can be deferred until after the fab is built. They are the critical path items that determine whether the fab can be built at all on the timeline that current policy commitments imply.

Unlike Scenarios 2 and 3, where a single legal reclassification, specifically Vietnam's removal from US strategic export control lists or Wassenaar-aligned compliance recognition, would unlock a decisive portion of the constrained value, Scenario 4 does not have a single resolution point. Its export control constraints are distributed across multiple jurisdictions, multiple equipment categories, and multiple ongoing procurement relationships that require their own resolution pathway. Progress on US bilateral standing reduces friction on US-origin equipment and Foreign Direct Product Rule exposure on third-country equipment. Progress on Dutch bilateral engagement reduces uncertainty on DUV lithography procurement timelines. Progress on Japanese equipment relationships reduces risk on deposition and etch tool supply. Progress on material supply diversification reduces operational vulnerability to Chinese material controls.

Each of these progress vectors is necessary, but none is individually sufficient. Scenario 4's relationship with the export control architecture is therefore not

one that can be resolved through a discrete policy achievement. It requires sustained, multi-front institutional engagement over the full construction and ramp timeline of the fab project. This is what makes Scenario 4 not just the most capital-intensive of the five scenarios but the most institutionally demanding, and why the quality of Vietnam's export control legal infrastructure is not a peripheral consideration for the Hoa Lac project but the foundational condition on which its feasibility ultimately rests.

Cross-Scenario Synthesis

The first and most consistent pattern is the convergence of all scenarios on the +1 pillar as the primary rate-limiting variable. Scenario 1's material vulnerability is ultimately a function of Vietnam's inability to credibly enforce US compliance requirements without triggering Chinese retaliation, a problem rooted in the absence of a recognized bilateral compliance framework. Scenario 2's die input chokepoint resolves primarily through VEU certification, which depends on Vietnam's host-country legal standing. Scenario 3's EDA tool and PDK access barriers are lifted most directly through legal reclassification within US and Wassenaar frameworks. Scenario 4's multi-jurisdiction equipment procurement problem requires bilateral institutional relationships whose quality depends on Vietnam's overall trust signal across the export control system. In each case, the technical and commercial constraints are real but secondary: the binding variable is the legal and institutional standing that determines what technology flows are permitted, at what cost, and with what degree of reliability. This convergence has a direct policy implication: investments in export control legal infrastructure are not sector-specific interventions that benefit one scenario at the expense of others. They are system-level investments that improve the conditions for all five scenarios simultaneously.

The second pattern is the asymmetry between how export controls affect different technology layers. The analysis reveals that controls operating at the equipment layer, as in Scenario 4, are the most difficult to resolve because they require multi-jurisdiction simultaneity and continuous compliance management over long time horizons. Controls operating at the input layer, as in Scenario 2, are more tractable because they concentrate at a single chokepoint that a specific legal reclassification can unlock. Controls operating at the software and IP layer, as in Scenario 3, occupy an intermediate position: they are more pervasive and compounding than input controls but more resolvable through institutional progress than equipment controls. And controls operating at the material layer, as in Scenario 1, are the least amenable to resolution through Vietnam's own policy actions because they depend on the bilateral dynamics between the US and China rather than on anything Vietnam does domestically. This asymmetry suggests that Vietnam's policy sequencing should prioritize the tractable before the institutionally demanding; resolving the software and IP access constraints of Scenario 3 and the input constraints of Scenario 2 through legal reclassification should precede, and will partially enable, the more complex multi-jurisdiction engagement that Scenario 4 requires.

The third pattern is that no scenario can be resolved through a single policy action, but some scenarios are more sensitive than others to a specific first move. Scenario 2 and Scenario 3 are both disproportionately sensitive to Vietnam's removal from US strategic export control lists and the associated progress toward trusted partner status: this single legal development would unlock VEU eligibility for advanced packaging die inputs and full-featured EDA tool access for chip design simultaneously, generating the largest cross-scenario impact of any discrete policy achievement currently within reach. Scenario 4 benefits from this development but is not unlocked by it alone. Scenario 1 benefits marginally and remains primarily exposed to material supply dynamics that legal reclassification does not directly address. Scenario 0 is the most resistant scenario to any single policy intervention because its persistence is structural rather than regulatory. Together, these three patterns point toward a recommendation architecture organized around institutional priority, policy sequencing, and differentiated engagement strategies for each of the four control regimes, which the following section develops in detail.

III. Policy Recommendations: A Realistic Assessment of Vietnam's Strategic Options

Realistic Scenario Positioning: What Vietnam Can and Cannot Credibly Pursue by 2030

The first act of realistic policy design is acknowledging that Vietnam's current institutional capacity supports credible pursuit of at most two of

the four non-baseline scenarios in the period through 2030, and that attempting to advance all four simultaneously would dilute resources and diplomatic attention to the point where none advances with sufficient speed to generate the track record and momentum that each requires.

Scenario 1, ATP hub consolidation, is already underway and does not require a strategic decision to pursue, it is the default trajectory of existing investments. The policy task here is not acceleration but protection: specifically, protecting the economic viability of existing ATP operations against the material supply vulnerabilities that China's export controls have introduced. This is a defensive priority, not a growth priority, and should be resourced accordingly.

Scenario 2, advanced packaging, is the highest-priority growth scenario for the period through 2030 for three reasons. First, capital investment is already committed and the facilities are already under construction, meaning the opportunity cost of not resolving the die input constraints is immediately measurable and politically visible. Second, the primary constraint, VEU certification and trusted partner status within the US export control framework, is more tractable than the multi-jurisdiction equipment problem of Scenario 4 or the compounding software access problem of Scenario 3. Third, progress on the +1 conditions for Scenario 2 generates spillover benefits for Scenario 3 simultaneously, making it the highest-leverage policy investment available.

Scenario 3, chip design hub, should be pursued as a parallel track to Scenario 2 but with realistic expectations about the timeline for generating commercially significant indigenous IP. The FPT PMIC export demonstrates proof of concept, but the distance between PMIC-level design and the chip architecture complexity that would generate defensible IP differentiation is substantial and cannot be closed by 2030 under any realistic training and technology access timeline. The policy task for Scenario 3 is therefore to establish the conditions for acceleration in the 2030 to 2035 period: building the compliance infrastructure that unlocks EDA tool access, creating the MPW and tape-out support programs that give design engineers real silicon experience, and initiating the reverse diaspora mechanisms that can import architect-level capability faster than the domestic training system can produce it.

Scenario 4, mature node foundry, should be acknowledged honestly as a post-2030 scenario in full form, even though the Hoa Lac groundbreaking has occurred. The multi-jurisdiction equipment procurement problem, the DUV lithography access uncertainty, and the material supply vulnerability combine to create a precondition set that cannot realistically be resolved on the timeline implied by the 2028 pilot production target without a level of diplomatic and institutional effort that would crowd out progress on Scenarios 2 and 3. The realistic policy task for Scenario 4 in the near term is not to accelerate the fab timeline but to establish the bilateral equipment access relationships and material supply buffers that make the fab viable when it does reach production readiness, and to manage political expectations about what the project can deliver by 2028 versus what it can deliver by 2032.

Concentrate Diplomatic Capital on the Single Highest-Leverage Action

Across the scenario analysis, one policy action generates more cross-scenario impact than any other: Vietnam's removal from US strategic export control lists and the associated progress toward trusted partner status within the BIS framework. This single development would unlock VEU eligibility for advanced packaging die inputs, materially improve EDA tool access for chip design, reduce the Foreign Direct Product Rule exposure on European and Japanese equipment for the fab project, and raise Vietnam's overall trust signal with Wassenaar member state technology suppliers simultaneously.

Vietnam should therefore concentrate its highest-quality diplomatic resources on this objective as the primary near-term priority, treating all other bilateral engagement tracks as supporting rather than parallel efforts. This means deploying senior-level engagement through the US-Vietnam Comprehensive Strategic Partnership framework specifically around export control reclassification, providing the US interagency process with concrete and verifiable evidence of domestic compliance infrastructure development, and accepting that the diplomatic bandwidth required for this track will limit what can be simultaneously pursued with the Netherlands, Japan, and South Korea in the near term.

The realistic expectation is that this reclassification process takes two to three years of sustained engagement to complete, meaning that the near-term policy task is to initiate and advance the process rather than to achieve its conclusion. Progress markers along the way, such as VEU applications for specific facilities, bilateral technology cooperation agreements with specific agencies, and formal BIS engagement on compliance infrastructure review, are themselves valuable signals to the market that Vietnam's trajectory is moving in the right direction even before formal reclassification is achieved.

Build Domestic Compliance Infrastructure to a Demonstrable Standard, Not a Legislative One

Decree 259/2025/ND-CP establishes a legal foundation, but the gap between a legal foundation and a compliance framework that Wassenaar member states and US BIS treat as credible is measured in enforcement track record, trained personnel, and verifiable process quality, not in the number of articles in a decree.

Vietnam should therefore prioritize the operational build-out of its compliance infrastructure over the legislative expansion of its legal framework. Specifically, this means establishing a functioning dual-use goods classification unit with personnel trained to Wassenaar standard methodology, creating a post-shipment verification program for controlled goods already in Vietnam that generates an auditable record of end-use compliance, and publishing transparency reports on export control enforcement decisions that partner country regulators can use as evidence of systemic rather than case-by-case compliance.

The realistic assessment here is that building this infrastructure to a demonstrable standard requires three to five years and a level of interagency coordination that Vietnam has not previously sustained on technology governance issues. The Ministry of Science and Technology, the Ministry of Industry and Trade, the Ministry of National Defense, and the Ministry of Public Security all have overlapping jurisdictions over dual-use goods management, and the absence of a clear lead agency with genuine enforcement authority is a structural gap that legislative text alone cannot fill. Establishing that lead agency, with adequate staffing and interagency authority, is a precondition for compliance infrastructure that generates the track record that diplomatic engagement requires.

Create Differentiated Engagement Tracks for Each Control Regime, Sequenced by Tractability

Given the bandwidth constraint identified above, Vietnam cannot run full-intensity bilateral engagement tracks with all four control regime jurisdictions simultaneously. The realistic sequencing, based on the tractability analysis embedded in the cross-scenario synthesis, should proceed as follows.

In the near term through 2027, the primary engagement track should be US BIS, for the reasons established in Recommendation I. The secondary track should be the Netherlands, specifically around DUV lithography access for the Hoa Lac project, because the timeline implications of delayed Dutch export licensing are immediate and the engagement required is bilateral and specific rather than multilateral and diffuse. These two tracks should receive the majority of available diplomatic and technical engagement resources.

In the medium term from 2027 to 2030, as progress on US and EU engagement generates compliance track record and institutional credibility, Vietnam should expand its engagement to Japan on deposition and etch equipment categories, and to South Korea on substrate and materials technology. These engagements benefit from the foundation built in the earlier period and are more likely to succeed when Vietnam can point to concrete compliance achievements rather than legislative commitments.

In the longer term from 2030 onward, Vietnam should pursue formal Wassenaar accession as its primary multilateral objective, using the compliance infrastructure and bilateral recognition built in the earlier periods as the evidentiary foundation for accession discussions. The realistic expectation is that Wassenaar accession is a 2030 to 2035 objective, not a near-term one, and policy planning should reflect this timeline rather than treating accession as imminent.

Accept and Communicate an Honest Strategic Positioning

The final recommendation is the one that policy documents most consistently avoid but that is

arguably the most important for Vietnam's long-term credibility as a technology partner: accepting and clearly communicating an honest strategic positioning that acknowledges what Vietnam is and is not in the near term. It is a country with genuine and growing strengths in ATP and emerging strengths in chip design that is navigating a complex multi-regime export control environment with institutional capacity that is adequate for some scenarios and insufficient for others. Communicating this positioning honestly, to US partners who need to trust Vietnam's compliance commitments, to EU partners who need to justify technology transfers, and to domestic stakeholders who need to calibrate expectations, is a precondition for the credibility that all of the other recommendations depend on.

The strategic positioning that the scenario analysis supports is specific and defensible: Vietnam as a trusted advanced packaging node and emerging chip design contributor in the Western-aligned semiconductor supply chain, with a longer-horizon aspiration toward mature node foundry capability that is being pursued responsibly within the constraints of its current institutional capacity. This positioning is honest, it is achievable, it is strategically valuable to Western partners seeking supply chain diversification, and it provides a clear framework for prioritizing the policy investments that the preceding recommendations identify. It is, ultimately, a more powerful position than the comprehensive semiconductor hub ambition that current policy documents sometimes imply, precisely because it is credible.

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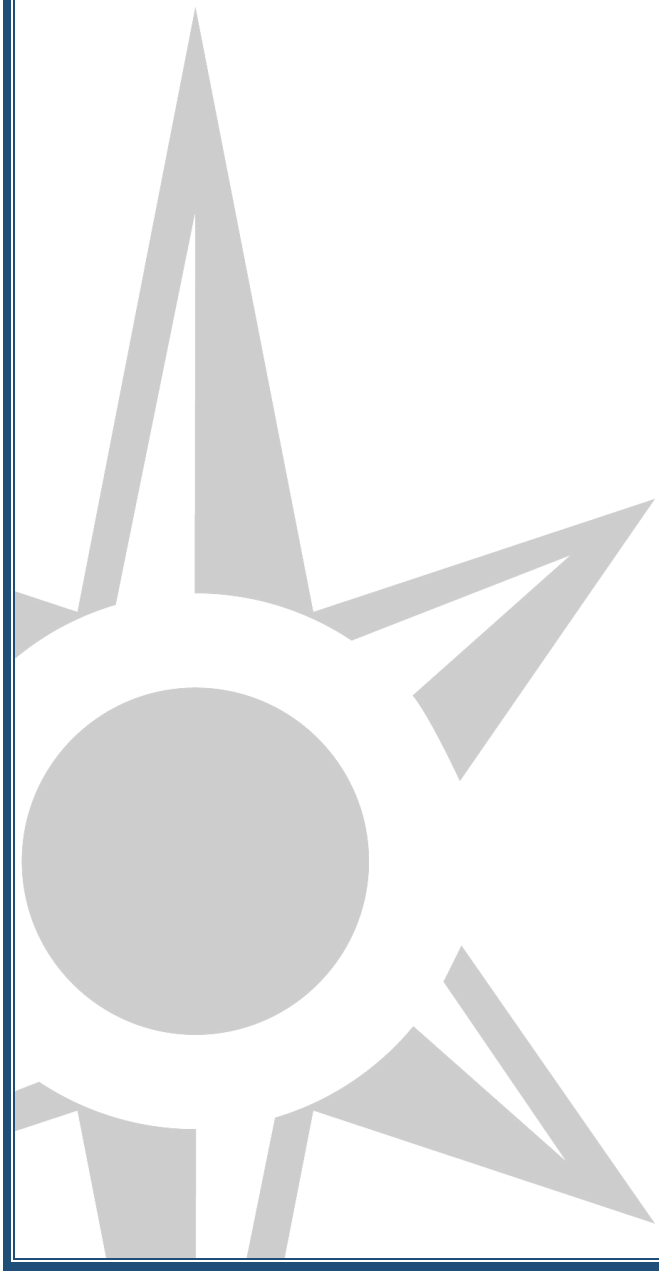
PACIFIC FORUM
INTERNATIONAL

Forging a Trusted Intellectual Property Framework for Vietnam's Semiconductor Industry

By
Trang Nguyen



Executive Summary

Trang Nguyen

In the complex and geopolitically charged landscape of the semiconductor industry, a nation's role is no longer defined solely by its manufacturing capacity or labor costs. It is increasingly determined by its trustworthiness and the security of its supply chain. For Vietnam, a nation strategically positioned between competing global powers and guided by the principles of "bamboo diplomacy," development of a robust and verifiable intellectual property framework is not a mere legal obligation but a strategic imperative. By moving beyond traditional compliance and adopting a comprehensive three-pillar framework, enterprises in Vietnam can transform from a low-cost manufacturing hub into a high value, secure, and reliable partner in the global semiconductor ecosystem, particularly with the United States (US).

The current legal and policy efforts in Vietnam, while progressive, are largely reactive to external pressures, such as the US tariffs, and are hampered by persistent enforcement deficiencies. To overcome these challenges, the proposed "Trusted Intellectual Property Framework" offers a roadmap built on three interconnected pillars:

Pillar I: Watermarking and Fingerprinting. This pillar establishes technical proof of ownership and a means to trace intellectual property infringement within the Outsourced Assembly and Testing sector, building confidence in Vietnam's manufacturing integrity.

Pillar II: Secure Split Manufacturing Protocols. Implementing technical protocols alongside a comprehensive legal and regulatory roadmap will address foundational issues of trade secret protection in a distributed supply chain. They ensure that high value know how remains protected throughout the manufacturing process, centered on collaborative environments with international partners.

Pillar III: Artificial Intelligence (AI)-based Intellectual Property Violation Detection. To complement existing measures and fulfill core requirements of a trusted framework, the enterprises should explore the potential of sophisticated technologies such as AI to detect intellectual property violations within complex design and development environments. Such an initiative could enhance internal enforcement capacity and signal a commitment to high standard protection.

By collectively implementing these pillars, the semiconductor companies operating in Vietnam will demonstrate its commitment to global standards through verifiable technological and legal mechanisms. This strategic integration aims to evolve intellectual property protection from a reactive compliance measure into a fundamental driver of national competitiveness. Ultimately, the proposed intellectual property strategies seek to contribute to establishment of a trusted ecosystem that fosters domestic innovation, secures international trust, and positions the nation as a reliable player in a highly contested global market.

Vietnam's Semiconductor Pursuits and its Strategic Ascension in the Global Landscape

As a critical arena for global competition, the semiconductor industry heavily influences the modern geopolitical landscape, where integrated circuits function as strategic assets for Artificial Intelligence (AI) and defense operations. Since global powers prioritize supply chain security, "trusted partner" status has become a fundamental requirement for international cooperation. Vietnam's participation in the world market depends on a direct link between intellectual property protection and national security. Developing a verifiable framework to support this connection is vital for a stable position in the high-tech sector.

New Geopolitical Landscape of Semiconductor Supply Chains

During three decades spanning from 1990 to 2020, the global semiconductor industry followed a rigid model of specialized comparative advantage, driven by cost-optimization and geographic concentration. Throughout that period, the United States (US) and Europe functioned as the primary innovation hubs, maintaining dominance in high value segments such as Electronic Design Automation (EDA), core processor architecture, and advanced lithography equipment. However, physical manufacturing underwent a massive migration toward East Asia. While Western firms transitioned toward capital light, "fabless" business models, East Asian nations leveraged aggressive state industrial policies to capture global manufacturing share. This shift began with Japan's dominance in memory chips during the 1980s, followed by the rise of the Taiwanese foundry ecosystem and South Korean leadership in memory and logic production. By 2020, this concentration resulted in a dramatic redistribution of global capacity, fundamentally reshaping the structural dependencies of the industry.

Region	1990 Market Share	2020 Market Share	Primary Focus Area
US	37%	12%	Design, EDA and Research and Development (R&D)
Europe	44%	9%	Automotive and Industrial Logic
Japan	19%	15%	Specialized Materials and Equipment
Taiwan	<5%	22%	Advanced Foundry (Logic)
South Korea	<5%	21%	Memory and Storage
China	<1%	15%	Mature Nodes and Assembly, Testing, and Packaging (ATP)

Table 1: Evolution of Global Semiconductor Manufacturing Capacity (1990-2020)
Source: Semiconductor Industry Association (SIA) & Boston Consulting Group (BCG), 2021[1]

The resulting highly efficient, "just in time" supply chain relied on a stable geopolitical environment where microchips were treated as high volume commercial commodities. During that era, intellectual property was viewed through a purely economic lens, serving as a tool for royalty collection and market competition rather than national security. This interdependence created a world where a single integrated circuit could cross international borders seventy times before reaching a final consumer. While the cost optimization model successfully lowered the price of global technology, it inadvertently created critical vulnerabilities. The emergence of China as a major downstream hub for ATP further complicated the landscape, setting the stage for the current shift toward a security first reconfiguration of global technology policy.

[1] Semiconductor Industry Association and Boston Consulting Group, *Strengthening the Global Semiconductor Supply Chain in an Uncertain Era* (April 2021), https://www.semiconductors.org/wp-content/uploads/2021/04/SIA-BCG-Report-2021-Strengthening-the-Global-Semiconductor-Supply-Chain.pdf.

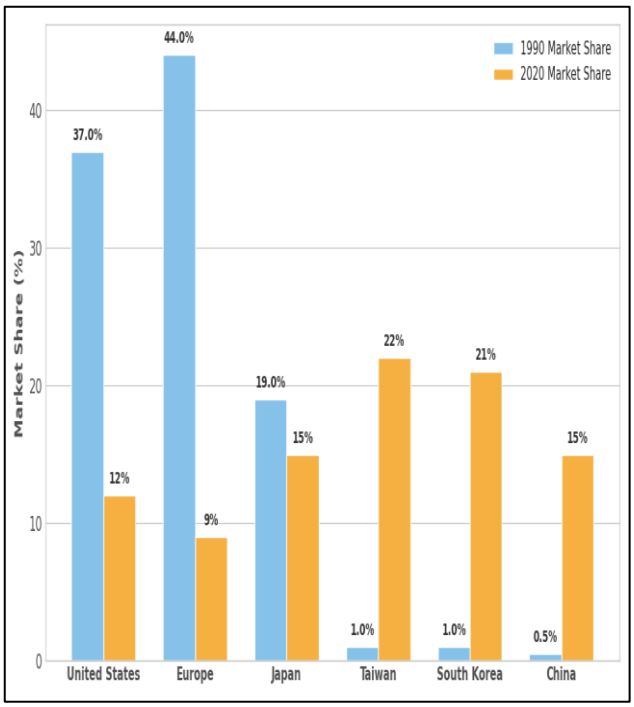


Figure 1. Global Semiconductor Manufacturing Capacity Evolution (1990 vs 2020)
Source: Semiconductor Industry Association (SIA) & Boston Consulting Group (BCG), 2021[2]

The vulnerability of the efficiency-first model became undeniable when the COVID-19 pandemic converged with intensifying strategic competition. This crisis exposed how extreme geographic concentration creates single points of failure, most notably when disruptions in a few localized hubs in East Asia paralyzed global automotive and industrial production. These events prove that a supply chain optimized solely for cost cannot withstand geopolitical or systemic shocks. Today, the industry is undergoing a fundamental transformation as nations abandon the concept of a unified global market in favor of a fractured landscape defined by de-risking and regional resilience. Control over semiconductor chokepoints now functions as one of critical components influencing national power, forcing a structural reconfiguration of the global value chain.

The US has utilized the CHIPS and Science Act of 2022 to reshore advanced logic fabrication while coordinating with international partners to restrict the flow of high-end technology. Simultaneously, the European Union leverages its specialized dominance in lithography equipment, led by ASML in the Netherlands, to establish technological sovereignty and secure its own industrial logic supply. Japan is now executing a rapid strategic comeback by providing massive subsidies to attract leading edge foundries and revitalize its domestic materials and equipment sector. Meanwhile, Taiwan and South Korea continue to hold the most critical positions in advanced fabrication, navigating a complex Silicon Shield strategy where their technological indispensability serves as a deterrent against regional instability.

In response to these Western-led restrictions, China is pivoting toward dominating legacy nodes while securing the upstream supply of critical raw materials such as gallium and germanium, creating new dependencies for global downstream industries. This strategic divergence accelerates the rise of a "friend shoring" model, a policy where supply chain networks are restricted to a circle of trusted nations with shared values and security interests. Friend shoring mitigates the risk of economic coercion by ensuring that production of sensitive technologies remains within a politically aligned group. This shift benefits emerging hubs within the ASEAN region and beyond. Malaysia solidifies its role as a global leader in ATP, while Vietnam, India, and Poland emerge as major recipients of relocated investment. India attracts significant interest for both ATP and compound semiconductor fabrication, while Poland becomes a strategic destination for leading edge assembly operations in Europe.

Nation / Entity	Strategic Focus	Global Role
US	Advanced Logic and EDA	Innovation Architect and Reshoring Hub
Europe	Lithography and Industrial Logic	Equipment Gatekeeper and Sovereign Clusters
Japan	Specialized Materials and Logic	Re-established Manufacturing Powerhouse

[2] Semiconductor Industry Association and Boston Consulting Group, *Strengthening the Global Semiconductor Supply Chain in an Uncertain Era* (April 2021), https://www.semiconductors.org/wp-content/uploads/2021/04/SIA-BCG-Report-2021-Strengthening-the-Global-Semiconductor-Supply-Chain.pdf.

Taiwan / South Korea	Leading edge Fabrication	Foundational Foundry and Memory Hubs
China	Legacy Nodes and Raw Materials	High volume Foundation and Upstream Control
Emerging Hubs (Malaysia, Vietnam, India, Poland etc.)	ATP and Design Diversification	Secure Downstream and Friend shoring Nodes

Table 2. Regional Strategic Focus (2022–2024)
Source: Semiconductor Industry Association (SIA), 2024 State of the Industry Report (2024)[3]

This reconfiguration elevates intellectual property protection to a security mandate. In a fragmented supply chain where high value designs are shared across borders within friend shoring circles, the target surface for industrial espionage, reverse engineering, and hardware level interference expands. The integrity of the design-to-foundry pipeline is no longer merely a corporate concern but a cornerstone of national defense. Consequently, the transition from labor-intensive ATP to high value design requires more than physical infrastructure; it necessitates a verifiable legal and technical framework capable of protecting core innovations against next generation threats.

The global semiconductor landscape faces further fragmentation as nations prioritize "sovereign ecosystems" over deep global integration. By the end of this decade, the success of current reconfiguration depends significantly on AI's evolution, which drives a massive demand for high performance computing. This surge has the potential to move new materials and advanced 3D packaging technologies into the geopolitical spotlight.

A notable shift is also anticipated toward open-source architectures, specifically Reduced Instruction Set Computer V (RISC-V). RISC-V functions as an open standard instruction set architecture that allows designers to develop custom processors without the burden of expensive licensing fees or the risk of export restricted proprietary technologies. Unlike traditional architectures controlled by single entities, RISC-V is maintained by a global non-profit organization based in Switzerland, making it an attractive neutral alternative. As countries seek to diminish their reliance on Western intellectual property, RISC-V offers a strategic pathway toward achieving technological self-sufficiency.

The transition introduces new challenges regarding the security and enforcement of intellectual property in emerging friend shoring networks. Intellectual property protection is poised to evolve from a corporate legal matter into a technical barrier used to maintain national competitive advantages. As chip designs become increasingly complex and find their way into narrower friend-shoring circles, establishing common standards for authentication and design copyright may prove decisive for the sustainability of technology alliances. The supply chain shows little sign of returning to its former centralized globalized state; instead, it is set to operate as a network of interconnected clusters based on shared security interests and political trust.

A Foundation in Motion: Vietnam's Existing Legal and Policy Efforts

Vietnam currently positions itself as a critical node in the global microelectronics value chain, leveraging its "bamboo diplomacy," an official foreign policy characterized by firm principles of self-reliance and tactical flexibility[4], to navigate the US – China strategic competition. This strategic positioning is formalized through the "C = SET + 1" formula, a conceptual blueprint enshrined in the National Strategy on Semiconductor Industry Development until 2030 (Decision No. 1018/QD-TTg).[5]. "C" represents Chips, while "SET" encapsulates Specialization, Electronics, and Talent, with the "+1"

[3] Semiconductor Industry Association, *2024 State of the Industry Report: Navigating Geopolitical Uncertainty* (May 2024), https://www.semiconductors.org/resources/2024-state-of-the-industry-report/.

[4] Ministry of Foreign Affairs of Viet Nam, "General Secretary Nguyen Phu Trong: An Outstanding Leader with Remarkable Contributions to Elevating Viet Nam's Diplomacy," July 20, 2024, https://mofa.gov.vn/web/ministry-of-foreign-affairs/detail/chi-tiet/general-secretary-nguyen-phu-trong-an-outstanding-leader-with-remarkable-contributions-to-elevating-vietnam-s-diplomacy-53.html.

[5] "Govt Targets to Raise Turnover of Semiconductor Industry to $100 Billion by 2050," *Bao Chinh Phu* (VGP News), Sept. 23, 2024, https://en.baochinhphu.vn/govt-targets-to-raise-turnover-of-semiconductor-industry-to-us100-billion-by-2050-111240923114027879.htm.

designating Vietnam as a premier secure and reliable alternative for global semiconductor operations. Far from being mere rhetoric, Vietnam's ambition is supported by a massive legislative watershed in 2025, during which the National Assembly approved a package of ten laws designed to modernize the nation's innovation architecture.[6].

The current policy shift reflects a transition from an investment model focused on labor intensive assembly toward one centered on high value intellectual capitalization and technological sophistication. Such a reform is anchored by the Law on Science, Technology and Innovation (No. 93/2025/QH15),[7], which introduces a "risk acceptance" mechanism. By granting administrative immunity to enterprises and research entities that follow established protocols, the law mitigates legal risks inherent in high-stakes semiconductor development, which is a vital assurance for any enterprise seeking to relocate sophisticated R&D activities to Vietnam.

The Amended Law on High Technology (No. 133/2025/QH15)[8] officially reclassifies semiconductor design, fabrication, and advanced packaging as "prioritized high technologies". This reclassification grants enterprises access to the highest tier of corporate tax exemptions, streamlined customs "green lanes" for sensitive equipment, and preferential land use rights.

To address the critical need for secure knowledge transfer, the Amended Law on Transfer of Technology (No. 115/2025/QH15) [9] introduces enhanced legal protections for "horizontal technology transfer,", specifically incentivizing the secure sharing of core intellectual property between partners in the supply chain, ensuring that trade secrets and other intellectual assets are shielded by rigorous non-disclosure mandates and civil remedies.

The Amended Law on Standards and Technical Regulations (No. 70/2025/QH15) [10] empowers enterprises to take a leading role in harmonizing Vietnam's technical benchmarks with international quality standards. This alignment ensures that locally produced chips meet the rigorous reliability requirements of global industries without facing technical barriers to trade. Together with the Digital Technology Industry Law (No. 71/2025/QH15), [11], which provides a "legal sandbox" for testing advanced designs, and the AI Law (No. 134/2025/QH15), [12], ensuring that AI assisted chip optimization remains within a verifiable ethical and legal framework, these reforms collectively aim to narrow the gap in intellectual property rights enforcement that previously hindered the attraction of front-end wafer fabrication.

In the global semiconductor value chain, core technologies, complex machinery, manufacturing processes, trade secrets, and semiconductor integrated circuit layout designs constitute the most critical intellectual assets. Such elements not only determine survival and competitive advantage of individual enterprises but are also inextricably linked

[6] "10 Laws on Science and Technology Adopted in 2025," *Vietnam Law Magazine*, November 15, 2025, https://vietnamlawmagazine.vn/10-laws-on-science-and-technology-adopted-in-2025-76350.html.

[7] National Assembly of Vietnam, *Law No. 93/2025/QH15: Law on Science, Technology and Innovation*, June 27, 2025, https://english.luatvietnam.vn/lawonsciencetechnologyandinnovationno93-2025-qh15datedjune272025ofthenationalassembly-405696-doc1.html.

[8] National Assembly of Vietnam, *Law No. 133/2025/QH15: Law on High Technology*, Nov. 30, 2025, https://datafiles.chinhphu.vn/cpp/files/vbpq/2026/01/luatso133.2025.qh15.pdf.

[9] National Assembly of Vietnam, *Law No. 115/2025/QH15: Law Amending and Supplementing a Number of Articles of the Law on Technology Transfer*, December 10, 2025, https://english.luatvietnam.vn/law-no-115-2025-qh15-dated-december-10-2025-of-the-national-assembly-amending-and-supplementing-a-number-of-articles-of-the-law-on-technology-transf-422298-doc1.html.

[10] National Assembly of Vietnam, *Law No. 70/2025/QH15: Law Amending and Supplementing a Number of Articles of the Law on Standards and Technical Regulations*, June 14, 2025, https://english.luatvietnam.vn/lawno70-2025-qh15datedjune142025ofthenationalassemblyamendingandsupplementinganumberofarticlesofthelawonstandardsandtechnica-405697-doc1.html.

[11] National Assembly of Vietnam, *Law No. 71/2025/QH15: Law on the Digital Technology Industry*, June 14, 2025, https://english.luatvietnam.vn/lawonthedigitaltechnologyindustryno71-2025-qh15datedjune142025ofthenationalassembly-405695-doc1.html.

[12] National Assembly of Vietnam, *Law No. 134/2025/QH15: Law on Artificial Intelligence*, December 10, 2025, https://english.luatvietnam.vn/law-no-134-2025-qh15-dated-december-10-2025-of-the-national-assembly-on-artificial-intelligence-422299-doc1.html.

to national foundational technology strategies and basic interests. To this end, building an effective intellectual property management mechanism within each enterprise; which covers all stages of defining what the company expects to gain from the management of its intellectual assets, determining the specific role that intellectual property can play in support of company's business, as well as selecting and pursuing a strategy to meet these objectives; is a prerequisite for building trust with international partners.

The Law Amending and Supplementing Several Articles of the Law on Intellectual Property (No. 131/2025/QH15),[13], hereinafter the 2025 Amended Intellectual Property Law, was passed by the National Assembly on Dec. 10, 2025, and will enter into force on April 1, 2026. A notable amendment in the general provisions is the addition of Article 8a., which affirms that intellectual property rights are assets that can be valued, traded, transferred, contributed as capital, or used as collateral. Clearly recognizing the proprietary nature of intellectual property rights is not merely a matter of legislative technique; it provides a vital legal basis for commercialization, capital mobilization, and the handling of security assets in business practice. This serves as legislative leverage, enabling domestic and international fabless chip design companies to mobilize capital and scale production without relying on traditional physical assets.

The pace of innovation in the semiconductor industry has been driven by Moore's Law, the principle that the number of transistors on a microchip doubles approximately every two years. However, as the physical limits of silicon materials are reached, Moore's Law is showing signs of slowing, forcing enterprises into an even more intense race to optimize architectures and manufacturing processes. To support businesses, Vietnam's Intellectual Property Law has maintained a specific mechanism under Clause 2 of Article 114, whereby semiconductor integrated circuit layout designs do not undergo substantive examination, ensuring a rapid right establishment process. Regarding patents, the 2025 Amended Intellectual Property Law significantly shortens their substantive examination period under Clause 2a) of Article 119 from 18 months to 12 months. Notably, in cases specified by the government, applicants have a right to request an expedited substantive examination with a timeframe of only three months for patents. Shortening these legal milestones allows critical semiconductor technical solutions to secure rights early, granting enterprises a market advantage before competitors can launch similar products.

In parallel with protecting the rights of owners, and to address long-term semiconductor human resource challenges, the 2025 Amended Intellectual Property Law maintains and clarifies exceptions for research and training under Article 125. This provision allows universities and R&D centers to use protected intellectual property for testing, analysis, and teaching purposes without such use being considered an infringement. The rationale for maintaining this exception is to foster academic freedom, allowing students and researchers direct access to the most advanced technological architectures. As a result, Vietnam can accelerate the training of high-quality semiconductor engineers, creating an abundant human resource supply to meet the rigorous demands of the global semiconductor industry.

For intellectual assets not registered via formal processes, trade secrets serve as a key form of protection, encompassing technical information such as doping processes or the detailed configuration of production machinery, which are often kept confidential to avoid disclosing core technology. The 2025 Amended Intellectual Property Law significantly strengthens this mechanism through Article 127, tightening measures against the illegal access of trade secrets, particularly acts that breach Non-Disclosure Agreements. A consequence of strictly enforcing such regulations is the creation of a transparent business environment where unauthorized access or information leaks within the supply chain are subject to severe sanctions. It is especially vital for protecting an enterprise's technological exclusivity during collaborative manufacturing or technology transfer activities.

To enhance enforcement efficiency in the digital era, Article 198b. of the 2025 Amended Intellectual Property Law, in coordination with Articles 42 and 45 of the Digital Technology Industry Law (No. 71/2025/QH15), standardizes the "Notice and

[13] National Assembly of Vietnam, *Law No. 131/2025/QH15: Law Amending and Supplementing Several Articles of the Law on Intellectual Property*, December 10, 2025, https://datafiles.chinhphu.vn/cpp/files/vbpq/2026/01/luat131-2025.pdf.

Takedown" mechanism.[14]. In the semiconductor industry, EDA files are the most sensitive assets, containing the entire logical structure and technical secrets of a chip. When the leak or unauthorized distribution of these EDA files occurs online, rights holders can issue a notice requiring intermediate service providers, including internet service providers and cloud storage platforms, to remove the infringing content immediately without waiting for lengthy court rulings. The mechanism provides a "quick response shield" that prevents widespread global damage and protects the integrity of intellectual assets, a key factor that reassures leading chip design corporations when establishing major R&D centers in Vietnam.

Such proactive legal overhaul is yielding concrete dividends, signaling a state of "verified readiness" to the global market. The influx of industry leaders is a direct response to Vietnam's evolving ecosystem, which prioritizes a streamlined manufacturing environment, rapid legislative modernization, and a commitment to transparent, secure administrative procedures. A hallmark of this trend is Amkor's US$($)1.6 billion project in Bac Ninh; during its initial phase ($520 million), the facility focuses on advanced System-in-Package assembly and testing solutions for the world's premier semiconductor and electronics firms.[15]. Intel has also implemented a significant strategic shift by migrating ATP operations from South America to Vietnam.[16] Combined with the $200 million AI factory partnership between NVIDIA and FPT[17] and the strategic presence of firms like Hana Micron, Marvell, and Lam Research, these developments confirm that Vietnam has successfully moved beyond the initial exploration phase. The nation is steadily maturing its capabilities to become a reliable, high trust partner in the global supply chain while fostering its internal foundations for technological autonomy.

However, the legal framework is one half of a complex trust equation. While robust legislation provides a necessary deterrent against infringement, it remains a reactive mechanism that addresses violations after they occur. As Vietnam seeks to integrate into exclusive "friend shoring" circles, where the sharing of high value semiconductor secrets is reserved for the most reliable partners, the government recognizes that legal mandates must be reinforced by proactive international technical standards. Relying solely on judicial recourse is insufficient in an industry where a single intellectual property leak can compromise a multi-billion-dollar architecture. Therefore, the strategic shift toward global technical benchmarks is not only an administrative upgrade but also a foundational necessity to ensure uncompromising security of high value proprietary technologies deployed within the country. By embedding security at the technical layer, Vietnam aims to provide continuous verification of its integrity, moving from promises of policy to a certainty of standardized execution. The comprehensive alignment of human capital, highlighted by the ambitious national goal to train 50,000 semiconductor engineers by 2030,[18], is intended to technically harden the nation's infrastructure. The viability of this target remains a formidable challenge though; falling short would prolong reliance on underqualified or external personnel, thereby expanding the attack surface for intellectual property leaks. Ultimately, overcoming such challenges represents an essential evolution from a low-cost assembly site to a strategic partner capable of safeguarding intellectual property integrity throughout the entire value chain.

[14] "Vietnam Amends Intellectual Property Law: Key Changes for Businesses," *Vietnam Briefing* (Dezan Shira & Associates), Dec. 23, 2025, https://www.vietnam-briefing.com/news/vietnam-amends-intellectual-property-law-key-changes-for-businesses.html.

[15] "Second Semiconductor Plant in North Begins Operations," *Government News* (VGP), October 11, 2023, https://en.baochinhphu.vn/second-semiconductor-plant-in-north-begins-operations-111231011162614755.htm.

[16] "Intel Reveals Plans to Expand Operations in Vietnam," *Vietnam Investment Review* (VIR), October 26, 2024, https://vir.com.vn/intel-reveals-plans-to-expand-operations-in-vietnam-139498.html.

[17] "FPT to Shape the Future of AI and Cloud on a Global Scale in Collaboration with NVIDIA," *FPT Software*, April 23, 2024, https://fptsoftware.com/newsroom/news-and-press-releases/press-release/fpt-to-shape-the-future-of-ai-and-cloud-on-a-global-scale-in-collaboration-with-nvidia.

[18] Prime Minister of Vietnam, *Decision No. 1017/QD-TTg: Approving the Program on Human Resource Development for the Semiconductor Industry until 2030, with a Vision to 2050*, September 21, 2024, https://english.luatvietnam.vn/cong-nghiep/decision-1017-qd-ttg-2024-program-on-development-of-human-resources-for-the-semiconductor-industry-through-2030-366646-d1.html.

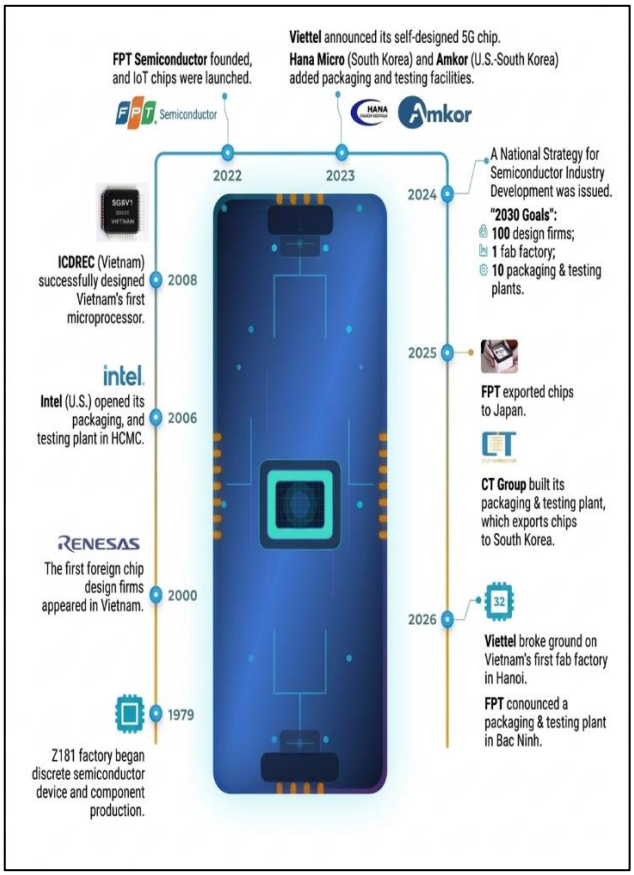


Figure 2. Vietnam's Semiconductor Industry Development Milestones (1979-2026)
Source: VnExpress[19]

The United States Context: Necessity of a "Trusted Partner" Framework

Washington appears to be transitioning its semiconductor strategy from cost efficiency toward a paradigm of national security primacy. Central to this shift is asymmetric competition, a strategic environment where national power rests on managing critical technological dependencies. To maintain such an asymmetric lead, the US must ensure that rivals can neither replicate American and allied technological advancements nor circumvent geopolitical restrictions. Within this evolving landscape, distinguishing between conventional trade partners and "Trusted Partners" now carries paramount importance, thereby prompting heightened emphasis on two critical issues: Intellectual Property Protection and Export Control Compliance.

Such a framework appears necessitated by the inherent vulnerability of semiconductor value chains to technology leakage. Unlike traditional manufacturing, sectoral value remains concentrated within design phases, most notably intellectual property encapsulated in chip architecture and EDA tools. Potential compromise of such intellectual assets, whether through unauthorized replication or industrial espionage, could rapidly erode Washington's primary technological advantages. This concern is codified in the CHIPS and Science Act of 2022,[20], a federal statute providing approximately $52.7 billion to bolster domestic research and manufacturing while imposing strict national security "guardrails" on technology sharing.[21]. Within such a legislative context, Intellectual Property Integrity, defined as the assurance that assets remain uncorrupted, authorized, and traceable throughout their lifecycle, is emerging as a critical benchmark for evaluating investment viability. Protecting intellectual property appears no longer merely a matter of corporate profitability; rather, it functions as a defensive measure to forestall reverse engineering by adversarial actors.

Operationalizing trust involves a sophisticated regulatory apparatus governed by Export Administration Regulations. One pivotal mechanism entails the Strategic Trade Authorization, which assigns nations to specific tiers based on perceived reliability. Tier 1 (Country Group A:5) status is generally reserved for "closest allies,", potentially allowing the transfer of dual-use technologies, possessing both commercial and military applications without individual licenses[22]. Conversely, technologies capable of enhancing rival

[19] "Những dấu mốc của ngành bán dẫn Việt Nam" [Milestones of Vietnam's Semiconductor Industry], *VnExpress*, Sept. 22, 2024, https://vnexpress.net/nhung-dau-moc-trong-ba-nam-cua-nganh-ban-dan-viet-nam-5012294.html.

[20] US Congress, *Public Law No. 117-167: CHIPS and Science Act of 2022*, August 9, 2022, https://www.congress.gov/bill/117th-congress/house-bill/4346/text.

[21] National Institute of Standards and Technology (NIST), "Fact Sheet: CHIPS for America Federal Incentives," April 2024, https://www.nist.gov/system/files/documents/2024/04/22/Fact%20Sheet%20-%20Federal%20Incentives-updated-508C.pdf.

[22] US Department of Commerce, Bureau of Industry and Security (BIS), "License Exception Strategic Trade Authorization (STA)," accessed June 2026, https://www.bis.doc.gov/index.php/documents/pdfs/2443-sta-compliance-guidance/file.

military capacities remain under stringent oversight. Any perceived failure to prevent the diversion of these items to entities on the "Entity List,"[23], such as Huawei or SMIC, likely invites severe sanctions or a suspension of technology transfers.

The US and Vietnam do not have a free trade agreement. Instead, bilateral economic and technological engagement is moderated by the Trade and Investment Framework Agreement and the Comprehensive Strategic Partnership established in 2023. While such a partnership signals political intent, the actual flow of sensitive technology appears contingent upon Vietnam's progression up the regulatory hierarchy toward Tier 1 status. Central to this progression is the International Technology Security and Innovation Fund,[24], authorized by the CHIPS Act of 2022, which explicitly prioritizes cooperation with nations demonstrating measurable progress in regulatory refinement and intellectual property enforcement. Without a verifiable framework to mitigate third party leakage, specifically scenarios where exported tools are surreptitiously re-exported to restricted markets, Vietnam's access to the American technological core may remain constrained.

The alignment between intellectual property protection and export control appears to constitute the foundation of "Trusted Partner" status. Whereas export control functions as a gatekeeper at the border, intellectual property protection serves as a guardian within the domestic industry. As Vietnam strives to enter this high trust zone, the nation faces the dual challenge of maintaining existing ATP capabilities while simultaneously preparing regulatory grounds for higher value design activities. Such a transition seems unlikely to be immediate; it requires a proactive alignment with US security standards. By addressing concerns regarding intellectual property theft and export diversion, Vietnam could derisk its semiconductor sector. Evidence suggests that the "Trusted Partner" framework is not merely a preference of Washington but a systemic requirement for any nation seeking deep integration into the US led microelectronics ecosystem.

Pillar I: Watermarking and Fingerprinting to Ensure Manufacturing Integrity

Challenges of Intellectual Property Infringement

The strategic integration of Vietnam into the global microelectronics supply chain, underpinned by significant foreign direct investment previously discussed in Section 2.2, has placed the nation at the center of distributed manufacturing models. However, as activities remain concentrated in the Outsourced Assembly and Testing (OSAT) sector, Vietnam enterprises face unique intellectual property risks that traditional protection mechanisms are struggling to address. Such challenges represent more than mere legal hurdles; they are strategic bottlenecks to Vietnam's pursuit of becoming a "Trusted Partner" in the global high-tech ecosystem.

Vulnerability in Outsourced Models and Data Leakage

In the semiconductor industry, sharing proprietary design blueprints with third party manufacturers creates significant security gaps. Primary challenges involve unauthorized overproduction and leakage of design data. Once manufacturing facilities possess technical specifications for a chip, there is a persistent risk of producing surplus units beyond original contracts to be diverted into illicit markets. Without technical means to verify the origin of each individual chip, original designers have virtually no way to distinguish between legitimate products and "ghost" units produced on their own contracted assembly lines.

Obsolescence of Reactive Enforcement in the Chip Era

Semiconductor sectors are defined by hyper accelerated product lifecycles where technological relevance is measured in months. While the 2025 Amended Intellectual Property Law provided a progressive legal framework, enforcement remains largely reactive, intervening only after violations have occurred. For any high-tech enterprise, pursuing multi year lawsuits often represents economic defeat even if they win legally, as infringed technology is likely obsolete by the time verdicts are reached. Such enforcement lags and complex judicial proceedings act as deterrents for global tech giants considering bringing high value designs to Vietnam.

[23] Cybersecurity & Infrastructure Security Agency (CISA), "Entity List," accessed June 2026, https://www.cisa.gov/resources-tools/resources/entity-list.

[24] US Department of State, "The International Technology Security and Innovation (ITSI) Fund," accessed June 2026, https://www.state.gov/the-u-s-department-of-state-international-technology-security-and-innovation-fund.

Forensic Barriers in Proving Infringement

Unlike traditional assets, proving that semiconductor chips have been illegally copied or physically tampered with is an expensive and technically daunting task. Current forensic processes often require invasive techniques, such as chemical delayering and microscopic cross sectioning, which physically destroy the chips, making it difficult to maintain evidence integrity for legal standards. Lack of self-verifying technical evidence embedded within products leaves intellectual property rights vulnerable to sophisticated copying techniques, ranging from structural reverse engineering to unauthorized physical modifications of device functions.

Consequently, relying solely on theoretical legal protection is insufficient to foster a trustworthy environment for international partners. To bridge the gap between innovation speed and legal inertia, the enterprises require a proactive defense mechanism, a technical shield that enables ownership verification and infringement detection directly from manufacturing stages, bypassing delays inherent in traditional litigation.

Technical-Legal Shield via Watermarking and Fingerprinting

To mitigate inherent delays of traditional litigation, a proactive framework must synthesize technical verification with legal recognition. This dual layered shield operates on a principle that evidence of ownership and authenticity should be irrefutable and self-contained within hardware itself. By embedding security protocols into semiconductor manufacturing cycles, Vietnam can move beyond reactive defenses toward models of continuous verification. Such integration ensures that technical data serves as a functional bridge between innovation labs and courtrooms, providing a foundation for trust in distributed production environments.

Hardware watermarking for Layout Design of Semiconductor Integrated Circuit

Watermarking involves insertion of unique, hidden digital signatures into layout designs of semiconductor integrated circuits. These marks are not merely labels but are woven into functional logic or physical geometries of a chip. Because such signatures are integral to circuit operations, attempting to remove or alter them would inevitably disrupt device performance or cause total failure. The indelible marks act as permanent records of intellectual property, allowing designers to assert ownership over specific layouts even when designs are illegally replicated. They accordingly provide primary evidence for identifying and protecting original layout designs against unauthorized reproduction.

Physical Unclonable Functions for Device-Level Authenticity

While watermarks protect layout-design, fingerprinting focuses on physical identities of individual units through Physical Unclonable Functions (PUFs). PUFs leverage microscopic, random variations inherent in silicon fabrication processes, functioning similarly to silicon DNA. No two chips are identical at the atomic level, and these variations allow for generation of unique cryptographic keys for every device. This capability is essential for IP protection as it enables designers to track chips throughout complex supply chains. By verifying these unique identities, authorities can instantly identify ghost production or unauthorized overproduction, as illicit products lack registered fingerprints generated at authorized factories.

Implementation of such sophisticated techniques does not require Vietnam to reinvent fundamental algorithms from scratch. Instead, feasibility lies in process compliance within existing OSAT facilities. Global industry leaders already established in the country, such as Intel, Amkor, Hana Micron etc. possess advanced manufacturing lines capable of integrating watermarking steps or PUF testing modules into standard production cycles. In this context, Vietnam serves as a strategic operator and supervisor, ensuring that security protocols meet international standards. Domestic engineers are capable of managing these encrypted systems through technology transfer and specialized training.

As the US seeks to diversify semiconductor supply chains through the CHIPS Act, Vietnam's adoption of the dual shield serves as a competitive advantage. By establishing a legal corridor for these tools, the nation signals its readiness to host high value designs. This proactive stance transforms intellectual property protection from a cost center into a strategic asset, positioning Vietnam as a secure and reliable alternative to traditional manufacturing hubs. Such

alignment ensures that technical solutions are supported by geopolitical cooperation, facilitating smoother technology transfer from global partners.

The strength of this technical shield is solidified by specific provisions in the Intellectual Property Law.[25]. Article 198 grants right holders' authority to apply technological measures for self-protection, effectively legalizing use of watermarks and PUFs as proactive defenses. More importantly, Article 203 recognizes digital data extracted from secure technical systems as direct evidence, shifting the burden of proof in infringement cases. When watermark data matches registered records, courts can establish a presumption of ownership, bypassing lengthy expert testimonies. Furthermore, synergy with the Electronic Transactions Law ensures that silicon fingerprints carry legal weight equivalent to digital signatures, providing robust traceability for every chip produced in the nation.

Watermarking and Fingerprinting Implementation for Manufacturing Integrity

To transition from theoretical concepts to industrial practice, Vietnam must establish a concrete roadmap for integrating watermarking and fingerprinting into its semiconductor ecosystem. This implementation strategy focuses on standardizing technical protocols, synchronizing digital evidence with legal registries, and incentivizing private sector compliance. By doing so, the nation can transform its manufacturing sites into high trust nodes that satisfy rigorous requirements of global supply chains.

Regulatory Framework for Hardware Security Benchmarking

Successful implementation requires a unified technical framework that defines acceptable standards for watermarking and PUFs. Enterprises should align their operations with international standards bodies to adopt benchmarks such as ISO/IEC 20243 for supply chain integrity. By providing a clear set of technical requirements, Vietnam ensures that various OSAT facilities operate under a synchronized security umbrella. Such standardization prevents fragmentation and allows for seamless verification of chips regardless of which facility performed assembly or testing.

Integration of Technical Evidence into Judicial Procedures

To empower the legal shield, Vietnam should develop a centralized digital repository. This system would allow designers to securely upload encrypted "watermark keys" during the registration of semiconductor layout designs. In event of a suspected infringement, authorities can retrieve these keys to perform non-invasive verification of physical units. Linking technical data directly to legal titles reduces administrative friction and enables "quick response" enforcement, effectively addressing the obsolescence risks.

Institutional Incentives for Verified Manufacturing Facilities

Industry consortiums should establish a "Trusted Node" certification for manufacturing facilities that demonstrate full compliance with advanced security protocols. Enterprises achieving this status could benefit from "green lane" customs procedures and priority access to government-backed R&D funds. This policy creates a market-driven incentive for firms like Intel, Amkor, and Hana Micron etc. to further invest in hardware-level security. Furthermore, certified facilities serve as a beacon for global fabless companies, signaling that Vietnam is a secure destination for high value designs.

Collaborative Technology Transfer and Talent Development

Realizing manufacturing integrity depends on a workforce capable of managing sophisticated encryption and testing modules. To achieve this, enterprises operating in Vietnam, regardless of their funding origins, must proactively drive collaborative technology transfer by establishing joint ventures and specialized training centers to disseminate watermarking and fingerprinting methodologies. This aligns with national goal of training 50,000 semiconductor engineers, ensuring that security is not just an imported feature but a core competency of local industry. By fostering a domestic ecosystem of security conscious engineers and onsite compliance professionals, Vietnam reinforces its position as a resilient and indispensable link in global chip network.

[25] National Assembly of Vietnam, *Consolidated Document No. 155/VBHN-VPQH: Intellectual Property Law* (Văn bản hợp nhất 155/VBHN-VPQH Luật Sở hữu trí tuệ), 2025, https://thuvienphapluat.vn/van-ban/So-huu-tri-tue/Van-ban-hop-nhat-155-VBHN-VPQH-2025-Luat-So-huu-tri-tue-672556.aspx.

Pillar II: Securing Trade Secrets in Split Manufacturing

While post fabrication mechanisms like watermarking and fingerprinting verify the authenticity of completed circuits, enterprises should consider securing their proprietary assets during the manufacturing process itself to establish a truly comprehensive defense.

For fabless design houses and technology integrators utilizing OSAT facilities, safeguarding process parameters, layout architectures and proprietary materials requires moving beyond conventional legal agreements. Pillar II outlines a strategic operational framework centered on secure split manufacturing protocols. By physically dividing production phases and coupling these technical barriers with rigorous contractual compliance, organizations can elevate their trade secret protection from abstract legal claims to empirically verifiable security measures.

Challenges of Trade Secret Leakage in Distributed Supply Chains

The structural reliance on external foundries presents a recognized challenge for semiconductor firms: commercializing an innovation requires sharing design blueprints with a third-party manufacturer. This transfer of proprietary data can introduce vulnerabilities, potentially exposing enterprises to risks such as industrial espionage, unauthorized overproduction, and reverse engineering.

From a legal perspective, these vulnerable design blueprints constitute critical trade secrets. Under Article 4.23. of Vietnam's current Intellectual Property Law [26], a trade secret is defined as information obtained from financial and intellectual investment that has not been disclosed and possesses commercial utility. When such valuable, undisclosed assets are transferred into a distributed manufacturing environment, they become subject to complex economic risks.

Overproduction and Intellectual Property Expropriation

Risk of trade secret leakage in outsourced manufacturing represents a foreseeable economic threat rather than merely a theoretical vulnerability. Analyses of buyer-supplier dynamics in semiconductor supply chains demonstrate that when a fabless firm transfers a complete design layout to a foundry, the foundry faces economic incentives to expropriate intellectual property through overproduction. Research on split manufacturing sourcing strategies indicates that in a single interaction between a design firm and a foundry without structural safeguards, the foundry may act in self-interest unless the design firm implements a split manufacturing strategy that distributes the manufacturing process across multiple independent foundries. By splitting chip design and production across independent foundries, this approach enables designers to manufacture their products while limiting any single foundry's access to complete design information, thereby reducing the risk of intellectual property theft.[27]

Without physical limitations in place, foundries possess the capability to run unauthorized "ghost shifts,", producing surplus identical units that are diverted to the gray market. The overproduced chips are manufactured on the exact same assembly lines using the original Graphic Data System (GDSII) design files. GDSII is the industry standard database format that serves as the complete physical and geometric blueprint of the integrated circuit. Such overproduced chips, therefore, are virtually indistinguishable from legitimate units. Detecting and proving overproduction remains one of the most complex challenges in modern supply chain management. The risk of expropriation deters investment and frustrates the negotiation of technology transfers, as buyers anticipate that suppliers will leverage the shared knowledge to bypass the original innovator.

Technical Vulnerability of Proximity Attacks

Even when enterprises attempt to obfuscate their designs before sending to a foundry, standard production methods leave hidden risks. This

[26] National Assembly of Vietnam, *Consolidated Document No. 155/VBHN-VPQH: Intellectual Property Law*, 2025, https://thuvienphapluat.vn/van-ban/So-huu-tri-tue/Van-ban-hop-nhat-155-VBHN-VPQH-2025-Luat-So-huu-tri-tue-672556.aspx.

[27] "Split Manufacturing Sourcing Strategy Under Risk of Intellectual Property Theft by Overproduction," *ResearchGate*; and "Inside the Supply Chain Trust Game," *Society Risk Analysis*, https://www.researchgate.net/publication/398954446*Split*manufacturing*sourcing*strategy*under*risk*of*intellectual*property*theft*by*overproduction; https://societyriskanalysis.libsyn.com/inside-the-supply-chain-trust-game.

vulnerability exists because chip design software operates in a highly predictable manner. To maximize speed and energy efficiency, the software automatically groups related components close together on the chip's base layer, which is the physical foundation where the microscopic switches, known as transistors, are built.

Such a predictable arrangement enables bad actors inside an untrusted factory to launch "proximity attacks". By observing how transistors are physically clustered on this base layer, they can use those physical clues to accurately guess how the missing wiring connections are supposed to link. It allows them to reconstruct the chip's overall logic. Hence, these physical clues show that software-level security is not enough when an adversary has direct access to the physical manufacturing environment.

Insufficiency of Contractual Deterrents

The escalating frequency of high-profile trade secret theft underscores the limitations of relying solely on non-disclosure agreements and standard legal deterrents. Recent industrial espionage cases highlight that vulnerabilities often stem from internal actors, misaligned supplier incentives, and the sheer volume of data transferred during production.

A stark realization of this risk occurred in the 2020 landmark case involving Taiwanese foundry United Microelectronics Corporation (UMC) and US-based Micron Technology. UMC pleaded guilty to criminal trade secret theft after its employees utilized "off-network" laptops to secretly access and transfer Micron's confidential dynamic random-access memory (DRAM) design rules, a critical technology used in memory chips, to a Chinese state-owned competitor. The US Department of Justice fined UMC $60 million, highlighting how traditional corporate firewalls fail when malicious insiders deliberately circumvent information technology (IT) detection systems.[28]

Similarly, the catastrophic breach suffered by Dutch semiconductor equipment maker ASML Holding NV demonstrates the devastating financial impact of trade secret misappropriation in the semiconductor sector. In 2019, ASML secured an $845 million judgment against US-based, Chinese-backed XTAL Inc. after former employees stole over 2 million lines of highly confidential source code. The stolen intellectual property was subsequently used to develop competing lithography optimization software. The damages awarded reflect the immense valuation of semiconductor trade secrets, yet the case emphasizes that post-breach litigation cannot restore the strategic exclusivity of compromised source code.[29]

Furthermore, data leakage is not always the result of coordinated corporate espionage; it frequently stems from negligent internal practices. For instance, in 2023, South Korean semiconductor manufacturer Samsung experienced significant data breaches when its engineers uploaded confidential semiconductor source code and meeting notes to public artificial intelligence chatbots in an effort to optimize the code.[30]

These occurrences indicate that generic organizational controls and standalone contracts are failing. When multi-billion-dollar designs are protected only by the threat of future litigation or standard employee handbooks, an asymmetry between cost of intellectual property theft and potential market reward heavily favors the adversary. So securing trade secrets requires moving beyond paper deterrents to structural, hardware-level defenses.

Technical Protocols as a Corporate Legal Shield in Split Manufacturing

Addressing the vulnerabilities of holistic outsourcing requires integrating security directly into the physical design process. Split manufacturing serves as a structural deterrent, significantly increasing the difficulty of reverse engineering while strengthening

[28] US Department of Justice, "Taiwan Company Pleads Guilty to Trade Secret Theft in Criminal Case Involving PRC State-Owned Company," Press Release, https://www.justice.gov/archives/opa/pr/taiwan-company-pleads-guilty-trade-secret-theft-criminal-case-involving-prc-state-owned.

[29] "Court Finally Awards ASML $845 Million in Damages and an Injunction," *Winston & Strawn LLP*, https://www.winston.com/en/blogs-and-podcasts/privacy-law-corner/court-finally-awards-asml-dollar845-million-in-damages-and-an-injunction.

[30] "Samsung ChatGPT Leak Details," *Mashable*, https://mashable.com/article/samsung-chatgpt-leak-details.

enterprises' evidentiary position in future trade secret disputes.

Mechanics of Split Fabrication

Modern microchips are built by stacking multiple physical layers, much like constructing a multi story building. Split manufacturing takes advantage of this architecture by deliberately dividing the production process into two isolated phases, handled by different factories. This ensures that no single supplier possesses the complete design information:

The Base Layer (Front-End-of-Line or FEOL): This initial phase builds the foundation of the chip, which contains billions of microscopic switches known as transistors. Because manufacturing these tiny components requires incredibly expensive, ultra-precise machinery, companies typically must outsource this step to high end global foundries.

The Wiring Network (Back-End-of-Line or BEOL): This subsequent phase adds the upper layers of microscopic wires that connect the isolated switches together to form a functioning processor. In a secure split manufacturing model, the unfinished chips are removed from the primary foundry before this upper wiring is added. The final wiring is then completed at a separate, trusted domestic factory or a rigorously vetted assembly partner.

By dividing the GDSII layout in this manner, the untrusted offshore foundry only produces a non functional "sea of transistors," a massive collection of disconnected switches. Without the final wiring map, the chip is useless; it cannot be tested, reverse engineered, or secretly overproduced for the gray market.

Logic Locking and Package-Level Routing Overlays

While separating the chip's layers is a foundational step, the ongoing threat of proximity attacks requires moving from passive separation to an active "logic locking" approach. Instead of merely cutting the connections, designers embed microscopic digital locks directly into the FEOL base layer. When this FEOL layer is manufactured, the chip remains mathematically locked and functionally useless until it receives a precise hardware key.

Crucially, the secret key is not stored in standard on-chip memory modules, which take up valuable space and are vulnerable to probing. Instead, the key is physically built into the wiring of the separate BEOL layer. For companies lacking a massive budget to operate a dedicated, trusted BEOL factory, a more cost-effective alternative can be used. This approach delegates an unlocking mechanism entirely to the final assembly and packaging stage. By extending the lock's connections to the chip's exterior pins and finalizing those connections at a trusted assembly facility, the company avoids the extreme costs of maintaining a trusted silicon factory. Because such a method does not require physically splitting the microscopic silicon layers, the chip can still be manufactured economically at an untrusted foundry, but its logic remains securely locked until it is placed into its final casing.

Translating Hardware Security into "Reasonable Measures"

The implementation of hardware-level security extends beyond physical protection; it serves a profound legal function in the context of trade secret protection. Unlike patents, which require public disclosure in exchange for a period of exclusivity, trade secrets are protected only as long as they remain confidential.

Under Article 84 of Vietnam's Intellectual Property Law[31], mirroring global standards such as the US Uniform Trade Secrets Act and China's Anti-Unfair Competition Law, proprietary information is only recognized and protected as a trade secret if it meets three simultaneous criteria: it possesses inherent confidentiality, it holds commercial value due to that secrecy, and the owner has taken "reasonable measures" or necessary means to safeguard its confidentiality.

In highly complex corporate litigation, the burden of proof rests heavily on the intellectual property owner to demonstrate that their security measures were commensurate with the value of the asset. Historically, enterprises relied on standard non-disclosure agreements (NDAs), data access logs, and password-protected servers to satisfy this requirement. However, as semiconductor espionage evolves and the digitization of trade secrets makes

[31] National Assembly of Vietnam, *Consolidated Document No. 155/VBHN-VPQH: Intellectual Property Law*, 2025, https://thuvienphapluat.vn/van-ban/So-huu-tri-tue/Van-ban-hop-nhat-155-VBHN-VPQH-2025-Luat-So-huu-tri-tue-672556.aspx.

extraction easier, courts are increasingly viewing static contracts and basic IT security as insufficient for protecting crown jewel assets, such as cutting-edge manufacturing parameters or proprietary design software. If an enterprise fails to exercise rigorous vigilance in protecting its data, courts can revoke its trade secret status entirely.

Hardware-level security fundamentally resolves this legal ambiguity. When a business physically divides its production logic across multiple facilities or utilizes package level logic locking, it provides compelling, empirical evidence of "reasonable measures". If an offshore foundry were to somehow reconstruct the intellectual property through an advanced attack and a lawsuit ensued, the business could demonstrate to the court that it engineered deliberate, capital-intensive structural barriers to prevent disclosure. By integrating active logic locking with split fabrication protocols, organizations transform subjective legal compliance into an objective engineering standard, significantly strengthening their evidentiary position in any subsequent misappropriation claims.

Defensive Paradigm	Technical Implementation	Satisfaction of "Reasonable Measures" (e.g., Vietnam IP Law Article 84)	Vulnerability Profile
Traditional NDA and IT Security	Legal contracts, basic access control, digital encryption.	**Low to Moderate** Courts increasingly view static contracts as insufficient for highly sensitive semiconductor IP.	**High** Vulnerable to malicious insiders, untrusted foundries, and ghost shift overproduction.
Standard-Split Manufacturing	Physical division of the base layer (FEOL) and wiring network (BEOL) across separate facilities.	**High** Demonstrates significant financial and logistical commitment to maintaining IP secrecy.	**Moderate** Susceptible to advanced proximity attacks utilizing physical clustering clues.
Logic Locking with Package Level Security	Base layer (FEOL) locked via embedded digital keys, unlocked during final assembly and packaging.	**Robust** Provides physical proof of proactive IP protection, definitively shifting the judicial burden of proof.	**Significantly Reduced** Mitigates both proximity attacks and insider extraction, as no complete functional data file exists in one location.

Table 3: Enterprise Risk Management and Legal Defensive Postures
Source: Synthesized from global trade secret litigation precedences and intellectual property law frameworks

Enterprise Compliance and Execution of Split Manufacturing Protocols

The integration of split manufacturing often necessitates a careful reassessment of corporate governance, vendor management, and contract enforcement. Technological solutions alone may not fully secure a supply chain if the supporting administrative and legal frameworks are inadequate. Enterprises should adapt to an environment where corporate liability is increasingly applied to supply chain partners who fail to adequately supervise data handling.

Shifting Standards for Corporate Liability

The operational requirements for enterprise compliance are experiencing a notable shift, influenced by recent legal actions in Taiwan that may serve as a reference point for the global

semiconductor industry. In a prominent 2025-2026 case, the local subsidiary of Tokyo Electron (TEL), a major semiconductor equipment supplier, was indicted and fined NT$150 million (approximately $4.7 million) for its role in a trade secret leak involving TSMC's advanced 2nm process

technology.[32]. The primary defendant, a former engineer, was sentenced to 10 years in prison under the National Security Act and Trade Secrets Act.

Although the misappropriation was executed by an individual employee, the Intellectual Property and Commercial Court held TEL corporately liable, citing a lack of sufficient, proactive measures to supervise employee behavior. Prosecutors noted that TEL's internal control measures appeared to be "generic on paper" and lacked the "concrete managerial actions" necessary to safeguard highly sensitive data.

This verdict suggests a gradual shift in legal expectations: passive compliance frameworks and standard confidentiality policies may no longer be adequate defense strategies if companies fail to demonstrate active, continuous oversight of their data environments. As semiconductor processes are increasingly designated as national security assets, companies operating within these supply chains, whether as fabless designers, equipment makers, or OSATs in emerging hubs like Vietnam, are advised to establish stringent internal regulations. These frameworks should treat all client and proprietary data as critical assets, focusing on comprehensive risk mitigation, structural security measures, and strict managerial oversight to prevent leakage.

Contractual Safeguards in Split Manufacturing

Implementing a secure split manufacturing strategy requires companies to carefully update their manufacturing contracts. Relying on standard, pre-drafted partnership templates, frequently referred to as joint development agreements, can create a false sense of security. In a complex, fragmented supply chain, intellectual property provisions should explicitly define how data and physical assets are controlled. To align with the realities of split manufacturing, enterprises are advised to legally codify the following critical elements:

Ownership of Physical Production Equipment

Contracts should clearly specify that the enterprise retains full ownership of all customized physical tools used to print the chips, such as photomasks and molds, during both the base layer (FEOL) and wiring (BEOL) stages. Merely paying a factory to produce a chip does not automatically secure the underlying design rights. Therefore, agreements should require the immediate return or destruction of these custom tools upon contract termination to prevent suppliers from reusing them for competitors.

Strict Production and Usage Limits

Agreements should restrict the factory from using the enterprise's intellectual property for any purpose other than fulfilling authorized purchase orders. Implementing strict production caps and unit tracking measures help mitigate the risk of unauthorized overproduction and the diversion of chips to the gray market.

Extending Protections to Subcontractors

Assembly and testing partners usually manage complex logistics and may outsource specific tasks to third-party vendors. It is essential that the same intellectual property restrictions, access limits, and security requirements are legally extended to any subcontractor, ensuring there are no weak links in the confidentiality chain.

Ownership of Process Improvements

During production, a factory might discover new ways to optimize the manufacturing process or improve chip performance. Contracts should proactively address who owns these newly discovered improvements. Establishing clear rules for ownership or joint patent filing helps prevent suppliers from independently patenting new techniques based on the enterprise's foundational technology.

Implementing Continuous Oversight and Incident Reporting

Executing a split manufacturing strategy requires continuous operational oversight. Enterprises are advised to work closely with their supply chain partners, such as foundries and assembly facilities, to implement rigorous access controls. Personnel access to the base layer (FEOL) or wiring (BEOL) schematics should be strictly compartmentalized. Utilizing "need-to-know" principles helps ensure that no single engineering team possesses visibility across the entire design lifecycle.

[32] *CommonWealth Magazine*, https://english.cw.com.tw/article/article.action?id=4737.

Furthermore, modern corporate compliance involves implementing rapid reporting mechanisms for any irregularities. In response to recent data security incidents, many leading technology integrators have significantly expanded their data protection clauses into comprehensive agreements. These updated contracts typically specify that suppliers should report any suspected data security irregularity or unauthorized access attempt to the intellectual property owner within a defined, narrow timeframe, often 24 hours to 72 hours, without interrupting ongoing services.

By combining the physical separation of split manufacturing with robust contractual obligations, enterprises can build a highly resilient defense for their intellectual property. This dual layered approach helps demonstrate compliance with statutory "reasonable measures" requirements and significantly mitigates the risk of insider threats and unauthorized overproduction. Ultimately, such practices support the development of trusted partner frameworks for high technology manufacturing, establishing the enterprise as a secure operator capable of navigating the geopolitical complexities of the modern semiconductor ecosystem.

Pillar III: Artificial Intelligence-Based Intellectual Property Violation Detection

To cultivate a "Trusted Partner" ecosystem, it is recommended that enterprises augment their defensive strategies with a proactive, technology driven enforcement posture. AI defined in this context as computational systems designed to perform complex pattern recognition and logical deduction, presents a unique capability to monitor and detect intellectual property violations comprehensively across the entire semiconductor lifecycle. By integrating AI tools, the companies could potentially shift their intellectual property enforcement from a reactive legal necessity to a proactive, automated shield, protecting multiple categories of intellectual assets simultaneously and reinforcing confidence among international partners.

Verification Limits in High Volume Electronic Design Automation

To appreciate the necessity of AI in modern intellectual property enforcement, one may first consider the physical and digital realities of contemporary semiconductor development. The industry depends heavily on EDA, which refers to the highly specialized software platforms used by engineers to design, simulate, and validate electronic circuits.

Modern integrated circuits routinely contain billions of microscopic transistors. The finalized blueprint for these chips is typically formatted as a GDSII file, which functions as a massive, multi-layered digital map containing geometric coordinates for every single component on the silicon wafer. Historically, verifying whether a new chip design unlawfully incorporated a patented architecture or a competitor's proprietary layout required manual review by specialized engineers. However, manual verification appears to have reached its functional limits. Human auditors may not efficiently process GDSII files containing billions of polygons, nor can they manually trace the complex logic paths of a modern processor to determine structural similarities.

In a sector characterized by hyper-accelerated product lifecycles, an intellectual property dispute that requires years of manual investigation could render the contested technology obsolete before a legal verdict is ever reached. When global technology integrators consider relocating their advanced research and development centers, a primary concern is whether the host nation possesses the technical capacity to detect and investigate intellectual property theft within these exceedingly complex datasets.

Furthermore, the EDA environment itself represents a persistent and parallel vulnerability. Because EDA tools are sophisticated and costly, software piracy within the business-to-business sector is a pervasive issue. Industry analysts estimate that a substantial portion of global EDA software usage occurs via unlicensed platforms, with the commercial value of such unauthorized use potentially exceeding billions of dollars.[33].

Using unlicensed EDA tools not only violates international copyright laws but also compromises

[33] "The Quandary of EDA Software Piracy," *Design And Reuse*; and "Your Design Software May Be Pirated," *EE Times*, https://www.design-reuse.com/news/202520468-the-quandary-of-eda-software-piracy/; https://www.eetimes.com/your-design-software-may-be-pirated/.

the security of the designs themselves, as pirated software often lacks critical security updates, leaving unpatched vulnerabilities open for industrial espionage. Global enforcement agencies are increasingly monitoring for illicit EDA usage, as evidenced by a recent international settlement where penalties reached $140 million for unauthorized transfer and use of restricted EDA software.[34].

These physical and commercial constraints demonstrate that traditional, human-driven enforcement mechanisms may be inadequate for the current technological era. Overcoming verification limits points toward a need for automated, high speed analytical systems capable of processing vast amounts of non-linear data, a requirement that advanced AI appears uniquely positioned to fulfill.

Technical Mechanisms for Artificial Intelligence - Driven Proactive Defense

Integrating AI into the intellectual property enforcement framework does not seek to replace human legal judgment; rather, it involves deploying specialized algorithms as advanced diagnostic instruments. These systems can scan, compare, and identify anomalies across massive datasets, effectively triaging potential violations for human expert review. The following sub-sections detail specific AI methodologies and their application to different facets of semiconductor intellectual property protection.

Graph Neural Networks for Hardware Architecture Detection

One of the emerging technical advancements in detecting hardware intellectual property piracy involves the application of Graph Neural Networks (GNNs). To understand why GNNs are necessary, it is helpful to conceptualize how a microchip is structured. Unlike a text document that reads sequentially, or a standard photograph that is organized in a simple, flat grid, a circuit design is more like a highly complex, multi-layered city map. In this "map,", the electronic switches that perform logic act as the intersections, and the microscopic wires connecting them act as the roads. Standard machine learning models often struggle to analyze these tangled pathways. GNNs, however, are a specific branch of AI expressly designed to process and learn from such interconnected networks, referred to in computer science as "graphs".

When a company seeks to protect a circuit design, it feeds its hardware blueprint into this AI system. This blueprint might be written as high level behavioral code (Register Transfer Level, or RTL) or drawn as a highly detailed structural wiring diagram (Gate-Level Netlist, or GLN). To analyze these files, researchers have developed specific AI software programs, such as the open-source HW2VEC or GNN4IP tools. What such AI programs do is trace how data flows through the chip's intricate pathways. The AI then translates the complex physical layout into a unique, compact mathematical signature, essentially creating a digital fingerprint of the chip's core logic.

This digital fingerprint becomes crucial if a manufacturer suspects that an untrusted factory has stolen its design. Frequently, a malicious actor will misappropriate the intellectual property but slightly shuffle the physical layout or add useless "decoy" wires to hide the theft, a deceptive technique known as hardware obfuscation. But because GNN AI understands the fundamental logic of the circuit, meaning how the data "traffic" moves, regardless of the reshuffled layout, it can compare the fingerprints and still identify the stolen structure. Experimental models utilizing these AI tools have indicated a capacity to detect hardware piracy with promising accuracy, doing so in a fraction of the time traditionally required by human engineers. Exploring the adoption of such AI-based verification tools within internal compliance frameworks could assist businesses in establishing a rigorous, proactive defense against hardware piracy.

Artificial Intelligence-Assisted Source Code Review and License Compliance

Modern semiconductor products are not just physical hardware; they rely heavily on software. The internal programs that control a chip (firmware) and its embedded algorithms often consist of millions of

[34] "Cadence Pleads Guilty, to Pay $140 Million in US-China Sales Case," *Reuters*; and US Department of Justice, "Cadence Design Systems Agrees to Plead Guilty and Pay Over $140 Million for Unlawfully Exporting," Press Release, https://www.reuters.com/world/china/cadence-plead-guilty-pay-140-million-us-china-sales-2025-07-28/; https://www.justice.gov/opa/pr/cadence-design-systems-agrees-plead-guilty-and-pay-over-140-million-unlawfully-exporting.

lines of source code. Protecting this code from unauthorized copying, and ensuring it does not accidentally incorporate restricted third-party code, are vital parts of a comprehensive intellectual property defense.

When a software dispute arises, technical experts traditionally read through the code line-by-line to find copied sections. Today, AI platforms using Large Language Models (LLMs) are helping to streamline this exhaustive process. These AI tools can rapidly scan massive code libraries to trace how data and commands flow through the software. If a competitor steals proprietary code but changes the superficial details, such as renaming variables to hide the theft, the AI can look past cosmetic modifications. Much like recognizing a stolen story even if the character names are altered, the AI identifies the underlying logical structure and flags the similarities for human lawyers to review.

A related, and usually overlooked, vulnerability involves Open-Source Software (OSS). While open-source code is free to use, it comes with strict legal conditions. For example, if a developer inserts certain open-source components, like those governed by the GNU (General Public License) into their own commercial product, the license may legally require them to publish their entire proprietary source code for free, effectively jeopardizing valuable trade secrets.

Recent European case law illustrates the significant legal and commercial consequences that may arise from non-compliance with OSS license obligations. In 2024, the French telecommunications company Orange S.A. was found liable after using an open-source authentication tool without disclosing its modified source code as required under the applicable license, resulting in a Paris court ordering damages of more than $1 million (€900,000). In a separate 2024 decision, the German router manufacturer AVM was held to have breached its OSS obligations by providing source code without the technical scripts necessary for compilation, demonstrating that even relati vely minor omissions in compliance can lead to substantial legal liability.[35].

To manage the risks, enterprises are increasingly deploying AI-driven Software Composition Analysis (SCA) tools. Think of SCA as an automated ingredient scanner: it continuously reviews a company's software during development, automatically identifying any third-party code snippets and warning engineers about potential license conflicts before the product is manufactured or distributed. Integrating such automated scanners into standard corporate compliance routines could help technology firms avoid inadvertently triggering international copyright disputes.

Artificial Intelligence-Assisted Claim Mapping and Freedom-to-Operate Analysis

Before a semiconductor company invests heavily in manufacturing a new chip, it generally conducts a Freedom-to-Operate (FTO) analysis. This legal and technical process aims to ensure that a new product does not infringe upon existing, valid patents held by third parties. The semiconductor industry possesses a dense patent landscape, where a single processor may intersect with thousands of overlapping patent families governing everything from transistor geometry to power management.

AI technology, specifically Natural Language Processing (NLP), offers significant enhancements to FTO analysis. Traditional keyword searches in patent databases are often ineffective because patent attorneys deliberately use varied or obscure language to describe similar technologies. AI-assisted tools address this by analyzing patents semantically.

The AI decomposes the complex legal language of a patent claim into structured technical elements and cross-references them against the specifications of the proposed chip design. By generating semantic similarity scores across millions of patents simultaneously, the AI can map "white spaces," specific technical dimensions where no enforceable patents currently exist. This allows engineers to identify safe zones for innovation. Rather than providing a binary "yes" or "no" regarding infringement, AI claim mapping generates a graduated risk profile, visually clustering patents to alert engineers to high-risk areas and suggesting alternative design architectures early in the research phase.

Computer Vision for Trademark and Brand Integrity

[35] "Open Source License Compliance: Lessons from Two Landmark Court Cases," *FOSSID*, https://fossid.com/articles/open-source-license-compliance-lessons-from-two-landmark-court-cases/.

While patents and trade secrets protect the internal mechanics of a device, trademarks safeguard a manufacturer's commercial identity and reputation. The distribution of counterfeit components presents a notable challenge to global supply chains, as unauthorized facilities sometimes produce substandard chips and apply the logos of established brands without permission.

To mitigate this risk, businesses are increasingly adopting computer vision algorithms to automate the detection of trademark infringement. In practical terms, this technology functions as a large scale, automated visual screening system. Instead of having employees manually search through thousands of online listings, these visual AI tools continuously process image data across e-commerce platforms and online marketplaces. By examining photos of product packaging or the logos printed on the surface of a chip, the AI compares online image directly against the brand's official design. It looks for subtle visual inconsistencies, such as a slightly incorrect font, an improper color shade, or incorrect spacing that might indicate a forgery. If the AI spots a suspicious listing for microcontrollers carrying an unauthorized logo, it can immediately alert the brand owner, allowing them to request a prompt removal of the listing before the products spread further.

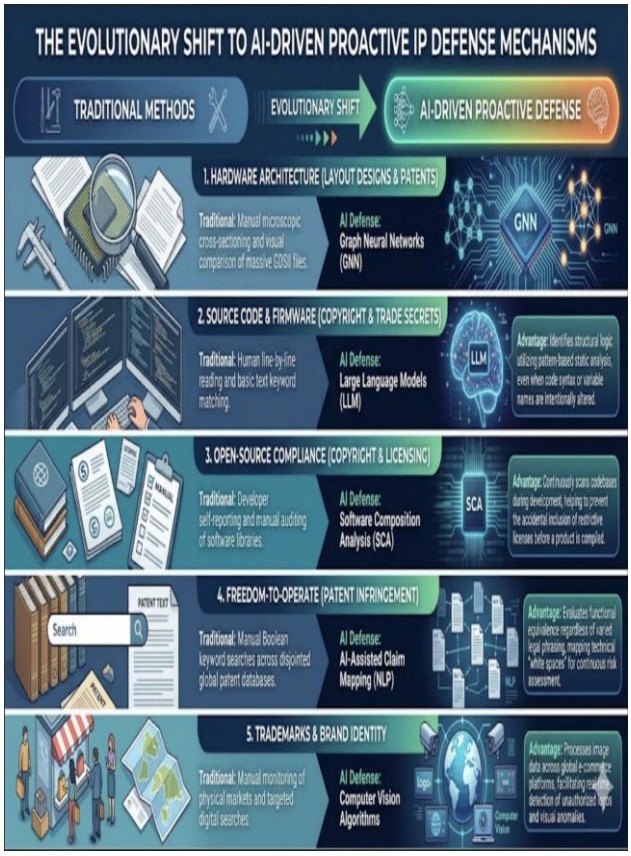


Figure 3. Comparative Matrix of Traditional vs. AI-Driven Intellectual Property Verification Mechanisms

Source: Author's compilation via Gemini (Imagen 3 Model)

Translating Artificial Intelligence Audits into Legal Defenses

Identifying a potential intellectual property violation via an algorithmic audit is an initial step in the enforcement process. To be actionable, these technical findings typically need to be converted into admissible legal evidence. As firms increasingly adopt these AI tools, it is helpful to evaluate how machine-generated data aligns with current statutory requirements and evidentiary standards.

Artificial Intelligence and Trade Secret Compliance

As discussed in Pillar II, maintaining trade secret protection, under Article 84 of Vietnam's Intellectual Property Law and similar international frameworks, requires the owner to implement "reasonable measures" to keep the information confidential. If an enterprise does not adequately secure its data, the information may lose its legal status as a protected trade secret.

The growing use of generative AI in daily business tasks introduces new considerations for this legal standard. When employees paste confidential data, such as chip architectures or internal pricing models into public, consumer-grade AI chatbots for quick summaries or code optimization, they are effectively transferring corporate secrets to a third-party server.

An illustrative example occurred in 2023 involving Samsung,[36], where engineers pasted confidential semiconductor source code into a public AI chatbot to check for errors. Sharing such information with an external platform lacking enterprise grade confidentiality agreements compromised the asset's secrecy. Similarly, in the 2024 US case West Technology Group v. Sundstrom,[37], complications

[36] "Samsung ChatGPT Leak Details," *Mashable*, https://mashable.com/article/samsung-chatgpt-leak-details.

[37] "Is Your AI Tool Quietly Destroying Your Trade Secrets?" *Troutman Pepper*, https://www.troutman.com/insights/is-your-ai-tool-quietly-destroying-your-trade-secrets/.

arose when an employee used a third-party AI transcription tool to record internal meetings, leading to unauthorized data retention after their employment ended. Following such incidents, courts have indicated a willingness to dismiss trade secret claims if a company uses public AI tools to process confidential data without proper safeguards, viewing such actions as a failure to meet the "reasonable measures" requirement.

On the other hand, deploying secure, internally hosted AI monitoring systems may support a company's legal defense. By using customized internal AI tools to oversee network activity, manage access to sensitive design files, and prevent unauthorized data transfers, a company automatically creates a detailed digital log of its security efforts. If there is an attempt to improperly download or share a chip design, these AI intervention logs can serve as objective evidence in court that the enterprise took active, reasonable steps to protect its data, thereby supporting the legal status of its trade secrets.

The Evidentiary Weight of Artificial Intelligence in Legal Proceedings

When pursuing legal action against a suspected infringer, the admissibility of AI-generated evidence presents new procedural questions. Courts generally hesitate to accept the output of a "black box" algorithm, a system that delivers a conclusion without explaining its internal reasoning, as standalone proof. A legal tribunal cannot impose liability based merely on an AI generating a broad similarity score, an aggregated percentage of likeness that fails to specify exactly which elements were copied. Instead, judicial standards demand granular, verifiable evidence. The AI system must demonstrate exactly *how* and *where* the infringement occurred, pinpointing specific files, structural overlaps, or copied lines of code etc. Without this transparent, line-by-line breakdown, a generalized AI assessment is unlikely to meet the standard of proof required in complex patent or copyright disputes.

To make AI audits legally actionable, the industry is increasingly adopting a "hybrid workflow" approach. In this setup, AI performs the initial data screening by scanning millions of lines of code or thousands of intellectual assets, but human technical experts curate the final assessment. For AI-assisted findings to be defensible in a courtroom, they require traceability and explainability, meaning attorneys must be able to demonstrate exactly how the AI arrived at its conclusion.

When an AI system flags a potential infringement, it typically generates a detailed "claim chart" or Evidence-of-Use matrix.[38]. This document maps the text of a patent claim to the corresponding technical features of the suspected product. In software disputes, the AI may identify the file paths and line numbers where the overlapping code is located. A human engineer or patent attorney then reviews these specific excerpts, confirms the technical context, checks for legal exceptions, and drafts the final expert report. By utilizing AI to pinpoint structural overlaps, legal teams can present objective, data-backed arguments. Within Vietnam's judicial framework, Article 203 of the 2025 Amended Intellectual Property Law[39] recognizes digital data extracted from secure technical systems as direct evidence. The provision appears to offer a supportive legal corridor for admitting such AI-generated, human-validated data into local courts.

Strategic Recommendations for Implementation

To fully actualize Pillar III, integrating AI-based detection capabilities into the broader semiconductor ecosystem is recommended. Moving beyond foundational legal updates, the operational deployment of AI tools by enterprises can serve as a verifiable indicator of the industry's commitment to supply chain security.

Establish "Digital IP Sandboxes."

The high cost of advanced EDA software and AI-driven compliance tools can serve as a barrier for local startups and academic institutions. Relying on unlicensed tools introduces notable legal and security vulnerabilities. It is suggested that industry consortiums, potentially supported by frameworks like the Digital Technology Industry Law, establish

[38] *Unified Patents*; and *Patlytics*, https://www.unifiedpatents.com/pearl; https://www.patlytics.ai/claim-charts.

[39] National Assembly of Vietnam, *Consolidated Document No. 155/VBHN-VPQH: Intellectual Property Law*, 2025, https://thuvienphapluat.vn/van-ban/So-huu-tri-tue/Van-ban-hop-nhat-155-VBHN-VPQH-2025-Luat-So-huu-tri-tue-672556.aspx.

centralized, cloud-based sandboxes. They could provide verified companies with facilitated access to legitimate EDA platforms integrated with AI-driven SCA and FTO tools. The shared infrastructure could help ensure that domestic design outputs are vetted for open-source compliance and patent non-infringement before entering the global market.

Clarify Guidelines for AI-Assisted Evidence

While the 2025 Amended Intellectual Property Law provides a progressive foundation, the mechanics of introducing AI-generated evidence into local courts could benefit from further clarification. The development of specialized evidentiary guidelines for high-technology disputes would be advantageous. Such guidelines might outline the requirements for "explainability" and "traceability" when submitting AI-generated claim charts, source code similarity metrics, or GNN circuit mappings. Establishing predictable rules for hybrid expert testimony could provide international partners with greater legal certainty.

Implement Standardized AI Literacy and Corporate Protocols

As demonstrated by recent corporate data leaks, the improper use of generative AI can compromise trade secret viability. It is advised that industry training initiatives incorporate cybersecurity and AI literacy modules. Furthermore, technology transfer agreements could encourage the implementation of internal corporate AI policies. By defining clear perimeters around the use of public AI models, the firms can better ensure they satisfy the "reasonable measures" threshold required by law in terms of trade secrets.

Proactive Geopolitical Positioning

In an environment where global stakeholders carefully evaluate the reliability of supply chain partners, local enterprises can leverage their implementation of AI-based IP detection as a strategic asset. By demonstrating that domestic facilities utilize automated AI auditing to help prevent unauthorized diversion of technology or the leakage of sensitive chip architectures, the industry provides verifiable indicators of its security integrity. This proactive transparency could facilitate deeper integration into the global, high trust microelectronics ecosystem.

Conclusion: A Strategic Intellectual Property Roadmap for Fostering Trust and Innovation

Synthesizing the Three Pillars

The strategic convergence of Watermarking and Fingerprinting (Pillar I), Secure Split Manufacturing Protocols (Pillar II), and AI-Based Intellectual Property Violation Detection (Pillar III) establishes a resilient, multifaceted defensive architecture for corporate enterprises operating within Vietnam. As the global semiconductor supply chain shifts toward security-oriented regional friend shoring networks, corporate reliance on passive, state-level judicial enforcement may no longer serve as an optimal or economically sufficient business strategy. The rapid pace of microelectronic innovation suggests that intellectual property protection should be integrated into the product lifecycle and monitored through appropriate algorithmic infrastructure.

For progressive companies, whether driven by foreign direct investment or backed by domestic capital mobilization, the integration of these three pillars provides operational coverage across various phases of supply chain vulnerability.

Pillar I secures the physical hardware asset post production, by leveraging the cryptographic features of PUFs for fingerprinting alongside hardware watermarks, chip firms can mitigate the economic incentives for unauthorized foundry overproduction and gray market diversion.

Pillar II addresses the security of the intellectual asset during the physical production phase. By executing physical split fabrication and deploying active logic locking, corporate entities seek to neutralize the risks of internal industrial espionage and proximity attacks at third party offshore foundries.

Finally, Pillar III monitors the digital and conceptual corporate perimeters; by deploying GNNs and SCA, enterprises can audit EDA datasets to ensure that proprietary source code is managed in compliance with restrictive, copyleft open-source licenses and protected against hardware obfuscation techniques.

Crucially, the integration of these three pillars extends beyond technical security. It helps satisfy the legal requirements for asserting trade secret viability. By implementing such security barriers, corporate companies generate a defensible trail of digital

evidence. Should cross border corporate litigation arise, the firm is better positioned to demonstrate that it executed the necessary "reasonable measures" to protect its core technological assets. This strategic posture can shift the judicial burden of proof from the corporate innovator toward the infringing party. In the context, integrating these three pillars transforms intellectual property protection from a reactive measure into a proactive competitive asset that generates corporate trust and market leverage.

Final Thoughts

While the proposed three-pillar framework addresses immediate supply chain vulnerabilities, a forward-looking intellectual property strategy must anticipate the industry's next evolutionary phases.

First, as Moore's Law decelerates, the focus of intellectual property protection will naturally expand from traditional transistor scaling toward safeguarding innovations in advanced 3D packaging and novel semiconductor materials.

Second, the anticipated shift toward open-source architectures, such as RISC-V, requires legal frameworks capable of securely managing collaborative innovation and modular licensing without compromising technological autonomy.

Finally, to sustain its position within friend shoring networks, Vietnam's techno-legal posture should remain agile, continuously adapting to emerging international security standards and the increasing integration of artificial intelligence in microchip design.

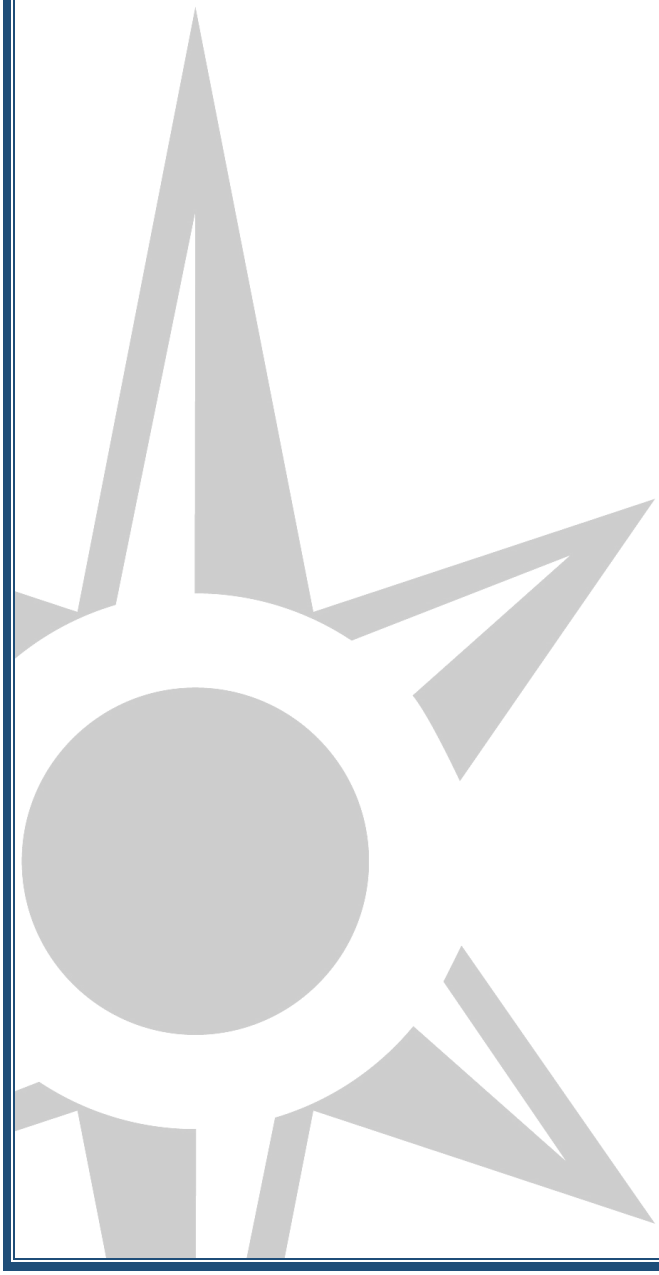
ABOUT THE AUTHOR

TRANG NGUYEN is an independent researcher based in Ho Chi Minh City, Vietnam. She began her career in Intellectual Property (IP) at the IP Office of Vietnam, where she spent a decade conducting research, providing legal counsel, examining industrial property applications, and leading public outreach. She later served as IP Coordinator at Rouse Legal and IP Counsel at Dentons, advising clients on IP enforcement, commercialization, and regulatory compliance. Most recently, she was Senior Research and Planning Officer at Fulbright University Vietnam, coordinating the IP and Technology Transfer Program sponsored by the U.S Department of State (Bureau of Oceans and International Environmental and Scientific Affairs). Trang holds degrees in International Relations, Corporate Finance, and an LL.M. in IP Law. Her current research focuses on strengthening Vietnam's semiconductor industry and innovation policy framework.

PACIFIC FORUM
INTERNATIONAL

Impact of Vietnam's Trade Export Controls (Decree 259/2025/ND-CP) on Vietnam's Semiconductor Industry: Policy Lessons and Recommendations for Strategic Export Controls

By
Tran Thi Mong Tuyen



Executive Summary

Tran Thi Mong Tuyen

This research examines how Decree 259/2025/ND-CP, issued in October 2025, impacts Vietnam's semiconductor and high-tech sectors, with a focus on protecting sensitive technologies, strengthening national security, and integrating into global technology supply chains. As Vietnam's first comprehensive legal framework for trading strategic goods, the decree defines dual-use and military-related technologies and encourages firms to implement Internal Compliance Programs (ICPs) to qualify for benefits such as long-term licensing. The study uses a qualitative, policy-focused methodology combining policy and document analysis, consultations with government agencies, engagement with Vietnamese academics, and discussions with multinational companies operating in Vietnam. It also considers the China Plus One strategy, assessing how multinational firms adjust investment and supply-chain decisions in response to Vietnam's regulatory environment.

Findings indicate that Decree 259 establishes structured mechanisms—including tiered risk-based licensing, streamlined procedures, domestic R&D oversight, alignment with international norms, and capacity building for compliance—that can help Vietnam safeguard strategic technologies, support national security, and facilitate integration into global high-tech networks. At the same time, the research highlights that realizing these benefits depends on effective implementation. Many domestic firms, particularly SMEs, face challenges in developing robust ICPs and navigating licensing processes. External pressures, including the ongoing US–China technology competition, regional trade rules, and transshipment considerations, further influence investment decisions and supply-chain integration.

Policy recommendations operationalize the concept of development-oriented strategic trade control, proposing measures to enhance predictability, strengthen compliance capacity, support domestic innovation safely, and ensure transparent guidance to investors. When implemented effectively, these measures create an environment in which domestic and multinational firms can invest, transfer technology, and innovate while balancing security objectives with industrial development goals. Decree 259 directly addresses the research question by providing a structured framework for protecting sensitive technologies, enhancing national security, and enabling Vietnam's semiconductor and high-tech industries to participate reliably in global technology supply chains. Its impact will depend on governance, capacity building, and proactive engagement with both domestic and international stakeholders. By pursuing a balanced and flexible approach, Vietnam can strengthen its role as a credible, resilient participant in regional and global high-tech networks.

Background

In October 2025, Vietnam issued Decree 259/2025/ND-CP, establishing the country's first comprehensive framework for regulating dual-use and strategically sensitive technologies[1]. The decree addresses export, re-export, temporary import, transit, and transshipment of strategic goods, including high-tech equipment with both civilian and military applications. Its implementation comes at a pivotal moment globally, as strategic export controls increasingly shape high-tech competition. For example, the United States has tightened restrictions on advanced semiconductors and artificial intelligence technologies to China, reflecting concerns over national security and technology transfer. Similarly, in January 2026, China reinforced export controls on certain dual-use technologies to Japan, demonstrating how major exporters use trade regulations to protect sensitive industries.

For Vietnam, these international developments underscore the dual challenge of safeguarding national security while enhancing credibility as a global investment destination. By establishing clear and enforceable rules for managing sensitive technologies, Decree 259 positions Vietnam as a trustworthy partner for multinational firms seeking high-value investment and technology transfer[2]. In a context where companies from Taiwan, South Korea, the United States, Japan, and China are diversifying production under the "China Plus One" strategy, a robust export control system signals Vietnam's ability to manage advanced technologies responsibly, comply with global trade standards, and protect intellectual property—all essential for attracting high-quality foreign direct investment (FDI) in high-tech sectors.

This study examines the potential implications of Decree 259 for Vietnam's semiconductor and high-tech industries, focusing on strategic technology management, national security considerations, and integration into global production networks. Drawing on policy analysis, international comparisons, and insights from industry stakeholders and confidential interviews, it identifies opportunities and challenges arising from the decree's licensing and compliance requirements, laying the groundwork for policy lessons on development-oriented strategic trade control.

It asks how Decree 259/2025/ND-CP will impact Vietnam's semiconductor and high-tech industries, particularly in terms of protecting sensitive technologies, ensuring national security, and integrating into global technology supply chains. Ultimately, it finds that implementation will determine effectiveness of the connections with global supply chains.

Research Methodology

This study adopts a qualitative, policy-focused approach to examine the impact of Decree 259/2025/ND-CP on Vietnam's semiconductor and high-tech sectors, with particular attention to balancing technology protection, national security, and integration into global supply chains. The research combines policy analysis, expert consultations, academic perspectives, and industry insights to capture multiple viewpoints, including those of government agencies, scholars, and multinational firms. First, a policy and document analysis is conducted, including a detailed review of Decree 259 and its related frameworks, such as Resolutions 57/NQ-CP, Resolution 59/NQ-CP, along with government reports, official publications, and academic literature, with a focus on dual-use and high-tech goods, licensing requirements, and compliance mechanisms. Second, the study engages in government consultations to explore the decree's impact on FDI, investment decisions, and compliance practices, as well as to understand the geopolitical rationale and Vietnam's efforts to position itself as a reliable partner for high-tech investment; all consultations are conducted in accordance with confidentiality and ethical standards. Third, perspectives are collected through comparative insights are drawn from Singapore, South Korea, Philippines, US, Taiwan's experience in export controls. Fourth, the study incorporates a China Plus One perspective, building on ongoing research to analyze how multinational firms adjust supply chains and investment locations in response to

[1] Báo Chính phủ. (2025, October 10). Chính phủ ban hành Nghị định về kiểm soát thương mại chiến lược. https://baochinhphu.vn/chinh-phu-ban-hanh-nghi-dinh-ve-kiem-soat-thuong-mai-chien-luoc-102251010181307612.htm

[2] Cổng Thông tin Bộ Công Thương. (2025, October 10). Chính phủ ban hành Nghị định về kiểm soát thương mại chiến lược. https://moit.gov.vn/chuyen-muc/chien-luoc-quy-hoach-ke-hoach-phat-trien/chinh-phu-ban-hanh-nghi-dinh-ve-kiem-soat-thuong-mai-chien-luoc.html

Vietnam's regulatory environment, providing a regional and geopolitical lens on high-tech sector development and FDI flows. Finally, all findings are synthesized and triangulated across policy documents, and consultations, with attention to the interplay between technology protection, national security, and global supply chain participation, in order to produce a balanced, realistic, and policy-relevant assessment of Decree 259's impact.

Literature Review

Decree 259/2025/ND-CP, issued in October 2025, represents Vietnam's first comprehensive framework for managing strategic goods. To date, there has been no research directly analyzing its impact, making this a timely topic. The decree can be understood in the context of Vietnam's recent policy initiatives, including [3] [4] on international integration and strategic goods management. The wave of 2025 policies reflects Vietnam's ambition to become a regional semiconductor hub and to strengthen its high-tech sector. Studying these policies presents challenges, as they are still in the early stages and many aspects are evolving. Analysis is further complicated by rapidly shifting global dynamics, including trade tensions, tightening export controls, tariffs, the China Plus One strategy, and broader geopolitical conflicts, all of which create uncertainty for policy implementation.

At the regional level, ASEAN's growing role as a manufacturing and high-tech hub makes it a competitive arena for major powers, also among ASEAN member states themselves, shaping both security and trade considerations. Drawing on literature on strategic trade control, high-tech FDI, and technology geopolitics, this research situates Decree 259 within both domestic and regional contexts. It provides insights into how Vietnam navigates the trade-offs between technology protection, economic growth, and geopolitical positioning.

Analysis

Vietnam's Decree 259/2025/ND-CP, which governs the export of dual-use and strategic technologies and took effect in October 2025, is a critical policy instrument for Vietnam's semiconductor and high-tech industries. To assess its impact, it is essential to consider three interrelated dimensions: protecting sensitive technologies, ensuring national security, and facilitating integration into global technology supply chains. This analysis examines these dimensions by situating Decree 259 within Vietnam's broader strategic and legal framework, the domestic industrial context, and regional and international experiences, highlighting both opportunities and challenges for implementation. These considerations are particularly important in light of the intensifying US–China technology competition, which has reshaped global supply chains and heightened scrutiny over high-tech exports and dual-use technologies.

Vietnam's export control regime under Decree 259 must be understood within the strategic context established by the Communist Party through Resolution 57 NQ/TW and Resolution 59 NQ/TW, issued in December 2024 and January 2025, respectively. Resolution 57 outlines Vietnam's ambition to achieve breakthroughs in science, technology, innovation, and national digital transformation, aiming for high-tech products to account for at least 50% of total exports [5]. It emphasizes the development and mastery of strategic technologies such as semiconductors, artificial intelligence, IoT, cloud computing, and digital infrastructure. Resolution 59 complements this vision by highlighting the country's commitment to international integration and strengthening the capacity of Vietnamese firms to participate in global

[3] Communist Party of Vietnam, "Resolution No. 57-NQ/TW on Breakthrough Development in Science, Technology, Innovation and National Digital Transformation," issued Dec. 22, 2024. The resolution establishes high-technology development, innovation, and digital transformation as central pillars of Vietnam's long-term economic modernization strategy.

[4] Resolution No. 59-NQ/TW on International Integration in the New Context," 2025. The resolution sets out Vietnam's orientation for deeper international integration, emphasizing proactive engagement in global economic, political, and security frameworks while strengthening resilience in supply chains and enhancing the management of strategic goods to safeguard national interests.

[5] Bộ Chính trị. (2024, December 22). Nghị quyết 57-NQ/TW về đột phá phát triển khoa học, công nghệ, đổi mới sáng tạo và chuyển đổi số quốc gia. Cổng thông tin điện tử Chính phủ Việt Nam. https://xaydungchinhsach.chinhphu.vn/toan-van-nghi-quyet-ve-dot-pha-phat-trien-khoa-hoc-cong-nghe-doi-moi-sang-tao-va-chuyen-doi-so-quoc-gia-119241224180048642.htm

markets while adapting to geopolitical and economic shifts. Together, these resolutions provide the strategic context in which Decree 259 operates, signaling that export control mechanisms should protect sensitive technologies while supporting innovation-driven growth, industrial upgrading, and global competitiveness. The geopolitical environment shaped by US–China competition further underscores the importance of these regulations, as Vietnam must navigate pressures to safeguard technology while remaining an attractive destination for foreign high-tech investment.

This strategic orientation has important implications for the implementation of Decree 259. Resolution 57 emphasizes institutional modernization, legal reform, and administrative simplification, creating conditions for export control procedures that are transparent, predictable, and aligned with industrial development priorities. For firms operating in sectors identified as national priorities—including semiconductors, advanced manufacturing, and digital technologies—licensing requirements, controlled item lists, and compliance procedures must protect sensitive technologies without unnecessarily constraining legitimate research, production, and export activities. Semiconductor manufacturers importing advanced machinery or components for assembly, for example, may fall under dual-use regulations, while AI-related technologies, though potentially dual-use, are central to Vietnam's digital transformation strategy. Effective implementation therefore requires a calibrated approach that addresses security concerns while enabling technological development, industrial upgrading, and export growth, particularly as Vietnam positions itself amid the global realignment of supply chains caused by US–China tensions.

Resolution 59 reinforces this perspective by emphasizing Vietnam's deeper integration into global value chains and alignment with international trade practices. Export control measures must support firms' participation in global markets, encourage foreign investment, and reduce regulatory uncertainty while safeguarding strategic technologies. This is particularly relevant in sectors such as semiconductors and digital platforms, where export controls intersect with complex international supply chains and trade agreements. Firms must navigate licensing requirements alongside broader trade considerations, including transshipment rules and potential tariffs under international agreements. Even compliant high-tech exports may be affected by these trade regulations, illustrating the broader operational and economic implications of Decree 259 beyond its legal provisions. The US–China technology competition adds an additional layer of complexity, as firms adjust sourcing, production, and export strategies to comply with international regulations while maintaining competitive access to key markets.

Vietnam's Decree 259 also operates within a wider legal and innovation ecosystem shaped by recent legislative developments, including the Law on Artificial Intelligence (effective March 2026)[6] and the amended Intellectual Property Law (effective April 2026)[7]. The AI law establishes a framework governing the development, deployment, and use of AI systems, emphasizing transparency, safety, human oversight, and risk management. While it does not directly regulate exports, it shapes the governance environment in which high-tech firms operate. Many AI-related technologies—from advanced processors to embedded AI components—may fall under dual-use classifications. By requiring governance and risk-management measures, the AI law encourages practices that complement the compliance and licensing requirements under Decree 259.

The amended Intellectual Property Law further strengthens this environment by reinforcing protections for technological innovations and clarifying ownership rights for AI-generated or AI-assisted works. Enhanced enforcement mechanisms, clearer protections for digital and partial designs, and alignment with international IP standards provide firms with greater certainty when commercializing advanced technologies. In sectors such as semiconductors, digital platforms, and AI applications, strong IP protection allows companies to document technology origin, demonstrate ownership, and ensure legitimate use—an important consideration when navigating export control requirements. Robust IP governance also facilitates

[6] Government News. (2026, July 15). *Viet Nam's Law on Artificial Intelligence*. https://en.baochinhphu.vn/viet-nams-law-on-artificial-intelligence-111260715113551787.htm

[7] Vu Nguyen Hanh. (2026, April 1). *Vietnam tightens intellectual property registration framework from April 1, 2026*. Vietnam Briefing. https://www.vietnam-briefing.com/news/vietnam-tightens-intellectual-property-registration-framework-from-april-1-2026.html/

participation in international supply chains, attracts foreign investment, and supports global competitiveness. Together, these legal developments create a regulatory environment in which export controls, technology governance, and intellectual property protection reinforce one another. They encourage responsible innovation while enabling high-tech firms to meet licensing requirements and expand their export activities. Viewed alongside Resolutions 57 and 59, Decree 259 forms part of a broader policy framework that integrates national security objectives with technological development, global integration, and responses to the US–China technology competition.

The implementation of Decree 259 is expected to have significant implications for Vietnam's semiconductor and high-tech sectors. Licensing requirements, ICPs, and multi-agency oversight will shape how sensitive technologies are accessed, transferred, and adopted domestically. In the short term, firms may experience adjustment costs, procedural delays, or increased compliance burdens, particularly in areas such as advanced lithography tools, high-performance integrated circuits, wide-bandgap materials (SiC/GaN), and electronic design automation (EDA) software. While these mechanisms are intended to protect sensitive technologies and mitigate security risks, they also create a structured framework for managing technology transfer and supporting the development of Vietnam's semiconductor ecosystem.

The Impact of Trade Policies

Beyond regulatory compliance, international trade rules may also affect how firms operate under the decree. Under Decree No. 292/2026/ND-CP [8] and current foreign trade frameworks, goods routed through Vietnam from third countries that undergo only minimal processing fail to achieve local origin status and are legally treated as non-originating transshipments. In the context of the pending US–Vietnam trade agreement, such goods could face tariffs of up to 40%[9], even if they comply with Decree 259 licensing requirements. This illustrates that export controls govern the legality and security of high-tech transfers, while trade and customs rules introduce additional operational and economic considerations that influence supply chain decisions and cost management. These trade implications are particularly salient as US–China tensions reshape sourcing and market access for high-tech products globally.

Vietnamese authorities have emphasized that strategic trade control, as formalized by Decree 259, is both regulatory and facilitative. By establishing clear rules and predictable procedures, the decree helps attract long-term, high-quality foreign investment that contributes to technological upgrading and domestic capability building. In 2025, Vietnam achieved a record level of FDI disbursement at $27.62 billion, 9% higher than 2024[10]. This trend suggests that investors increasingly value predictable regulatory frameworks that support high-value manufacturing and technological development.

The decree may also strengthen Vietnam's attractiveness to high-technology investors operating in sectors where technology governance, intellectual property protection, and regulatory compliance are increasingly important. Vietnam has already attracted major technology firms, including Intel, Samsung, Amkor Technology, Synopsys, Marvell Technology, and Nvidia, reflecting its growing role within regional semiconductor and electronics value chains. Insights from discussions with industry to Intel and Samsung suggest that strategic trade controls are becoming an increasingly important component of the investment environment for advanced technology industries. Industry perspectives emphasized that export controls differ fundamentally from sanctions: rather than targeting specific countries or entities, strategic trade controls focus on regulating sensitive technologies, dual-use items, and their potential end uses. Effective

[8] Government of Vietnam. (2026, July 22). *Decree No. 292/2026/ND-CP dated July 22, 2026, of the Government detailing a number of articles and measures for organizing and guiding the implementation of the Law on Foreign Trade Management*. LuatVietnam. https://english.luatvietnam.vn/decree-no-292-2026-nd-cp-dated-july-22-2026-of-the-government-detailing-a-number-of-articles-and-measures-for-organizing-and-guiding-the-implementat-441247-doc1.html

[9] Dezan Shira & Associates. (2025, September 25). *Transshipment and origin risks: What Vietnam-based businesses need to know to stay compliant*. Vietnam Briefing. https://www.vietnam-briefing.com/news/transshipment-origin-risks-vietnam-based-businesses-stay-compliant-2025.html/

[10] Chotimah, C. (2026, January 5). *FDI into Vietnam rises 9% in 2025*. Trading Economics. https://tradingeconomics.com/vietnam/foreign-direct-investment/news/514551

implementation therefore depends on clear product classifications, transparent licensing criteria, institutional capacity, and coordination among relevant government agencies.These discussions also highlighted the importance of maintaining a balanced approach. On the one hand, a credible export-control framework can demonstrate Vietnam's commitment to the responsible management of sensitive technologies, thereby strengthening confidence among international partners and investors. On the other hand, excessive regulatory burdens could undermine competitiveness and discourage investment. Industry representatives therefore emphasized the value of practical compliance mechanisms, including ICPs, clear guidance for firms, and risk-based licensing procedures that focus regulatory attention on genuinely sensitive technologies while facilitating legitimate commercial activities. In this regard, Decree 259 has the potential to support both technology security and continued participation in global semiconductor and high-technology supply chains.

From a technology protection perspective, Decree 259 links licensing approvals to firms that maintain robust Internal Compliance Programs[11] and subjects sensitive technologies to multi-agency review. The policy is therefore likely to encourage higher standards of technology governance and compliance among firms operating in strategic sectors. While multinational corporations typically maintain sophisticated export compliance systems, many domestic firms in emerging technology industries may have limited experience with export control procedures. As a result, the decree may incentivize firms to strengthen internal compliance capabilities, improve technology management practices, and develop greater awareness of technology security requirements. Experience from countries such as South Korea, Singapore, and the United States demonstrates that risk-based licensing frameworks—combining enhanced scrutiny for sensitive technologies with expedited approvals for low-risk items—can support both security objectives and industrial development. If implemented effectively, Decree 259 could similarly contribute to Vietnam's transition toward higher-value activities, advanced manufacturing capabilities, and stronger domestic technological capacity.

Beyond its regulatory and economic functions, Decree 259 also carries broader geopolitical implications in the context of intensifying great-power competition over critical and emerging technologies. As export controls become an increasingly salient tool of economic statecraft, the establishment of a formal strategic trade control framework signals Vietnam's growing awareness of the security dimensions embedded in global technology flows. Rather than being solely a domestic regulatory measure, the decree can be interpreted as part of Vietnam's effort to position itself as a responsible and predictable actor within an increasingly fragmented technological order. In a context where advanced semiconductors, dual-use technologies, and supply-chain nodes are subject to heightened scrutiny, the presence of a structured export-control regime helps reduce external uncertainty regarding Vietnam's role in sensitive technology circuits. At the same time, it reflects Vietnam's broader geopolitical strategy of maintaining strategic autonomy by avoiding overdependence on any single power while aligning with widely recognized international norms of technology governance. In this sense, Decree 259 contributes to shaping Vietnam's external positioning as a "trusted but non-aligned" participant in the evolving architecture of global technology regulation.

Challenges

At the same time, realizing these outcomes will depend on how effectively the decree is implemented. One of the most significant challenges concerns the uneven compliance capacity of domestic firms. While large multinational corporations often possess established export-control procedures and dedicated compliance teams, many Vietnamese small and medium-sized enterprises (SMEs) have limited experience with strategic trade controls, licensing requirements, and ICPs. As a result, compliance costs may fall disproportionately on domestic firms, potentially creating barriers to participation in high-value segments of semiconductor and technology supply chains. This challenge is particularly important because the long-term success of Vietnam's industrial upgrading strategy depends not only on attracting foreign investment but also on strengthening the capabilities of domestic enterprises

[11] Government of Vietnam. (2025, October 10). *Decree No. 259/2025/ND-CP on strategic trade control*. LuatVietnam.

and increasing their integration into global production networks.

A second challenge stems from the broader geopolitical environment. The ongoing US–China technology competition has accelerated the use of export controls, investment screening mechanisms, and restrictions on advanced technologies. Although Decree 259 may enhance Vietnam's credibility as a responsible participant in global technology supply chains, it also places the country within a more complex strategic landscape in which firms must navigate overlapping regulatory requirements from multiple jurisdictions. Changes in foreign export-control policies or technology restrictions may influence investment decisions, technology transfer arrangements, and supply-chain configurations in ways that are beyond Vietnam's direct control.

In addition, Vietnam's position within regional production networks creates practical implementation challenges. The semiconductor and electronics industries rely on highly fragmented cross-border supply chains, often involving multiple stages of production across different economies. Compliance with strategic trade controls therefore requires effective coordination among customs authorities, licensing agencies, manufacturers, and logistics providers. Issues related to transshipment, end-use verification, and regulatory interoperability may increase administrative burdens if procedures are not implemented consistently and transparently. The challenge is not simply to strengthen security oversight, but to do so without undermining the speed, predictability, and efficiency that make Vietnam an attractive destination for investment.
Addressing these challenges will require more than regulatory enforcement alone. Capacity-building programs for domestic firms, particularly SMEs, stronger inter-agency coordination, regular consultation with industry stakeholders, and continuous adaptation to technological and geopolitical developments will be essential to ensuring that Decree 259 supports both national security objectives and long-term industrial development.

Policy Recommendations

- Vietnam's export control regime under Decree 259/2025/ND CP can be strengthened through a risk-based licensing approach with strategic prioritization. While the decree already requires firms to obtain permits for dual-use and strategic technologies and offers extended 12-month licenses for companies with certified ICPs, a tiered licensing system could improve both efficiency and predictability. Under this approach, technologies would be classified according to their strategic sensitivity. Tier 1 would cover highly critical technologies, such as advanced semiconductor fabrication equipment, high-performance integrated circuits, and wide-bandgap materials like SiC and GaN, and would be subject to rigorous multi-agency review and enhanced ICP verification. Tier 2 would include mid-range electronics and precision instruments, following standard licensing procedures with routine ICP checks. Tier 3 would encompass low-risk consumer electronics, eligible for expedited licensing to reduce administrative friction. By focusing regulatory attention on the most sensitive technologies while facilitating trade in lower-risk items, this framework allows Vietnam to protect strategic assets without stifling industrial growth. It also provides multinational firms, particularly those relocating production from China under the China Plus One strategy, with the predictability needed to plan investments and maintain stable supply-chain operations. International experience, including the Wassenaar Arrangement[12] and Singapore's Strategic Goods framework[13], demonstrates that such tiered, risk-based licensing effectively balances security, trade facilitation, and industrial development. While intensive review of Tier 1 items may slow some investments, it strengthens technology protection, signals credibility to global partners, and encourages compliance among high-tech investors.

[12] Arms Control Association. (2022, February). The Wassenaar Arrangement at a glance. https://www.armscontrol.org/factsheets/wassenaar
[13] Singapore Customs. (2026, February 24). Permit and registration requirements overview. https://www.customs.gov.sg/permits-and-licences/trade-controls-and-prohibitions/strategic-goods-control/permit-and-registration-requirements/permit-and-registration-requirements-overview

- Alongside risk-based licensing, ensuring efficient and predictable implementation is critical to the effectiveness of Decree 259. For multinational firms pursuing China Plus One diversification strategies, transparency in licensing procedures and reasonable processing timelines can influence investment planning and supply-chain decisions. Conversely, lengthy procedures or regulatory uncertainty may reduce Vietnam's attractiveness relative to other destinations in Southeast Asia. To address these challenges, Vietnam could further streamline authorization procedures, strengthen appeal and review mechanisms, and expand the use of digital licensing and tracking systems. In pursuing these reforms, Vietnam can draw lessons from ASEAN countries, such as Singapore and the Philippines. Singapore's Strategic Trade Scheme (STS) provides a useful example of how trusted and compliant firms can benefit from more flexible licensing arrangements[14]. Through the use of bulk and global permits, Singapore reduces administrative burdens for both regulators and exporters while maintaining oversight of strategic goods and technologies. Elements of this approach could help Vietnam improve efficiency for firms with strong ICPs and established compliance records. The Philippines offers a different but equally relevant lesson. Since the adoption of the Strategic Trade Management Act (STMA) in 2015, the Philippines has gradually developed its strategic trade control system through phased implementation and institutional capacity building[15]. Coordination between licensing authorities, customs agencies, and economic zone administrators has helped reduce duplication and improve regulatory coherence. As Vietnam continues implementing Decree 259, similar efforts to strengthen inter-agency coordination and digital integration could facilitate compliance while reducing administrative complexity. By combining more flexible licensing arrangements for trusted firms with enhanced inter-agency coordination and digitalization, Vietnam can improve the efficiency and predictability of its strategic trade control regime without compromising national security objectives. Such measures would support investor confidence, facilitate participation in global semiconductor and high-technology supply chains, and reinforce Vietnam's position as a reliable destination for advanced manufacturing and technology-related investment.

- Building industry compliance capacity is equally important, particularly because many domestic firms lack experience with export control procedures. Offering guidance, training, and advisory services—especially to SMEs and multinational firms relocating production from China—can improve understanding of licensing obligations and ICP requirements. Firms with robust internal compliance programs experience fewer violations and integrate more effectively into global high-tech supply chains. While such training requires resources, the payoff is significant: reliable technology transfer, stronger supply-chain security, and sustained industrial growth. In the context of US–China competition, equipping domestic firms with compliance skills ensures that Vietnam can participate safely in global supply chains without inadvertently transferring sensitive technologies to unintended actors.

- Vietnam should also support domestic strategic capability while managing risks. Encouraging semiconductor R&D and production in critical processes—such as wafer fabrication, photolithography, and advanced packaging—can strengthen supply-chain resilience and reduce dependence on foreign suppliers. At the same time, firms must maintain strong internal compliance programs consistent

[14] Singapore Customs. (2026). Strategic goods control overview. https://www.customs.gov.sg/permits-and-licences/trade-controls-and-prohibitions/strategic-goods-control/strategic-goods-control-overview

[15] Republic Act No. 10697. (2015, November 13). An Act Preventing the Proliferation of Weapons of Mass Destruction by Managing the Trade in Strategic Goods, the Provision of Related Services, and for Other Purposes (Strategic Trade Management Act). Republic of the Philippines. https://lawphil.net/statutes/repacts/ra2015/ra_10697_2015.html

with Decree 259. Controlled, ICP-driven growth mitigates the risk of sensitive technology leaks while sustaining Vietnam's attractiveness to multinational investors. South Korea's approach under its Foreign Trade Act [16] illustrates how structured oversight can protect sensitive technologies while supporting legitimate industrial expansion. By developing domestic capabilities safely, Vietnam strengthens national security, enhances industrial competitiveness, and positions itself as a reliable partner in global high-tech supply chains, especially in a landscape shaped by US–China technological rivalry.

- To maintain agility in a rapidly evolving technological and geopolitical environment, Vietnam should institutionalize mechanisms for monitoring, evaluation, and policy adaptation. A permanent advisory body comprising government agencies, industry representatives, technical experts, and academic specialists could periodically assess investment trends, emerging technologies, and potential dual-use risks, while conducting scenario planning related to supply-chain disruptions and geopolitical developments. This is particularly important in the semiconductor sector, where rapid technological advances can quickly outpace existing control lists and licensing procedures. Similar to the European Union's practice of periodically reviewing and updating its dual-use export-control framework[17] [18], including control lists and implementation guidance in response to technological and security developments, such a mechanism would enable Vietnam to adapt licensing procedures, compliance requirements, and strategic goods controls to changing circumstances. Continuous evaluation would help ensure that Decree 259 remains effective, supports national security objectives, and maintains a predictable regulatory environment for domestic and foreign firms.

- Beyond strengthening domestic licensing and compliance mechanisms, Vietnam should also consider the regional dimension of strategic trade control. As Southeast Asia becomes an increasingly important destination for high-tech manufacturing and supply-chain diversification, governments across the region face growing pressure to ensure that dual-use technologies are transferred, used, and re-exported responsibly. At the same time, heightened geopolitical competition and expanding export-control measures among major powers have increased scrutiny of technology flows through third countries, including those in ASEAN. Given ASEAN's consensus-based decision-making model [19] and the diversity of its members' security and economic priorities, a binding regional export-control regime is unlikely to be feasible. Nevertheless, ASEAN can play a constructive role in promoting dialogue, confidence-building, and the exchange of best practices on strategic trade management [20]. Rather than pursuing harmonized regulations, ASEAN could consider issuing a high-level statement encouraging information sharing, capacity building, and voluntary cooperation on risk assessment and compliance related to dual-use goods and emerging technologies. The Philippines' 2026 ASEAN Chairmanship may provide a timely opportunity to advance such discussions. As one of the first

[16] Park, E. Y., Pak, J., Kim, J.-u. J., & Yoo, M. (2025). South Korea: Latest developments in evolving sanctions and export control framework. Global Investigations Review. https://globalinvestigationsreview.com/review/the-asia-pacific-investigations-review/2026/article/south-korea-latest-developments-in-evolving-sanctions-and-export-control-framework

[17] European External Action Service. (2022, July 25). Project 90 "Export control programme for dual-use goods – Southeast Asia" – Kick-off meeting. https://www.eeas.europa.eu/delegations/vietnam/project90_en

[18] European Commission. (n.d.). *Exporting dual-use items*. Directorate-General for Trade and Economic Security. https://policy.trade.ec.europa.eu/help-exporters-and-importers/exporting-dual-use-items_en

[19] Hussain, N. (2026, April 14). *ASEAN's economic agenda: Towards greater strategic agency?* RSIS. https://rsis.edu.sg/rsis-publication/rsis/co26079/

[20] ASEAN 2026 Philippines. (2026, May 12). *ASEAN Law Forum on export control opens, strengthens regional legal cooperation in criminal matters*. https://asean2026.gov.ph/post/view/?title=asean-law-forum-on-export-control-opens-strengthens-regional-legal-cooperation-in-criminal-matters

ASEAN member states to establish a comprehensive legal framework for strategic trade controls through the Strategic Trade Management Act (STMA) of 2015[21], the Philippines has accumulated valuable experience in regulating dual-use goods, strengthening compliance mechanisms, and engaging with international non-proliferation and export-control frameworks. Drawing on these experiences, ASEAN could facilitate exchanges among member states on regulatory practices, industry compliance, and emerging technology governance. Such an initiative would serve several important functions. First, it would demonstrate ASEAN's collective commitment to responsible management of sensitive technologies, reinforcing the region's credibility as a destination for high-value manufacturing and technology investment. Second, it would provide a platform for technical cooperation and policy learning while preserving the flexibility and sovereignty of individual member states. Third, enhanced regional communication could reduce regulatory uncertainty for firms operating across multiple ASEAN jurisdictions and strengthen the resilience of regional technology supply chains. For Vietnam, supporting greater ASEAN cooperation on strategic trade management would complement the objectives of Decree 259 and align with the broader goals of Resolution 59-NQ/TW on international integration. Participation in regional dialogue would reinforce Vietnam's commitment to international standards for strategic trade control while maintaining an open and predictable environment for investment, technology transfer, and industrial development. By linking domestic implementation with regional cooperation, Vietnam can further strengthen its reputation as a trusted and responsible partner in the semiconductor and broader high-technology sectors.

- Beyond ASEAN-level cooperation, Vietnam can further strengthen the effectiveness of Decree 259 by benchmarking its strategic trade control regime against established international practices. Rather than seeking full harmonization with any single model, Vietnam should selectively draw lessons from different sources that address distinct aspects of strategic trade management. The Wassenaar Arrangement[22] can serve as a reference for strategic goods control lists and multilateral best practices, while the US Export Administration Regulations (EAR)[23] offer useful insights into licensing procedures, compliance requirements, and enforcement mechanisms. In addition, the experiences of economies such as Singapore, South Korea, and Taiwan provide practical examples of how strategic trade controls can be implemented while supporting high-technology industries and maintaining international competitiveness. Taiwan offers a particularly relevant reference point. Despite not being a member of major multilateral export-control regimes, it regularly updates its strategic goods control lists and compliance procedures to remain aligned with international standards and maintain the confidence of global technology partners[24]. Vietnam could adopt a similar approach by periodically reviewing controlled-item lists, strengthening ICP requirements, and refining licensing procedures in response to technological developments and evolving international trade practices. Selective alignment with international best practices would provide several benefits. It would enhance regulatory credibility, facilitate participation in global semiconductor and high-technology supply chains, and provide greater certainty for

[21] Pabeliña, K. M. G. (2016). The strategic trade management regime in the Philippines. *Strategic Trade Review*, *2*(2), 118–129. https://strategictraderesearch.org/wp-content/uploads/2017/09/8.-The-Strategic-Trade-Management-Regime-in-the-Philippines.pdf

[22] Arms Control Association. (2022, February). The Wassenaar Arrangement at a glance. https://www.armscontrol.org/factsheets/wassenaar

[23] International Trade Administration. (n.d.). *U.S. export controls*. U.S. Department of Commerce. https://www.trade.gov/us-export-controls

[24] Taiwan News. (2026, February 12). Taiwan adds 18 high-tech items to export control list. https://www.taiwannews.com.tw/news/6301519

multinational firms operating in Vietnam. At the same time, Vietnam should retain sufficient policy flexibility to address national development priorities and protect emerging domestic technologies. Striking this balance would help reassure international partners that sensitive technologies are managed responsibly while supporting the broader objectives of industrial upgrading, technological innovation, and national security.

- Finally, transparent communication and engagement are essential. Clear guidance on licensing, ICP expectations, and the strategic rationale behind dual-use controls helps domestic and foreign firms navigate regulatory requirements efficiently. This is particularly important for companies relocating production from China. Transparent and consistent communication reduces delays, encourages technology transfer, and reinforces Vietnam's role in regional and global semiconductor and high-tech supply chains. By establishing trust and predictability, Vietnam signals that it can balance national security objectives with industrial development and global integration.

Collectively, these policy recommendations operationalize the concept of development-oriented strategic trade control, showing how Decree 259 can simultaneously protect sensitive technologies, strengthen national security, and facilitate industrial upgrading. When implemented effectively, these measures create a predictable, transparent, and capacity-driven environment in which domestic and multinational firms can innovate, invest, and collaborate. This positions Vietnam as a responsible, competitive participant in the global semiconductor and high-tech ecosystem, directly addressing the research question of how Decree 259 impacts sensitive technology protection, national security, and integration into global technology supply chains, while acknowledging the strategic pressures posed by the US–China technology competition.

Conclusion

Decree 259/2025/ND-CP establishes Vietnam's first comprehensive framework for regulating dual-use and sensitive technologies while supporting the development of the country's semiconductor and high-technology sectors. By introducing controls over strategic technologies, the decree seeks to reconcile national security considerations with industrial development and participation in global technology supply chains. The findings of this study suggest that the decree's impact will depend largely on implementation. Transparent and predictable licensing procedures, risk-based regulatory approaches, strong inter-agency coordination, and sustained capacity building will be essential to its effectiveness. This challenge is particularly significant for domestic small and medium-sized enterprises (SMEs), many of which have limited experience with export-control compliance but are expected to play an increasingly important role in Vietnam's industrial upgrading and integration into higher-value production networks. In addition, the implementation of Decree 259 will take place in an environment shaped by technological change, supply-chain restructuring, and intensifying geopolitical competition.

The decree creates an opportunity for Vietnam to strengthen its governance of strategic technologies while maintaining an open and competitive investment environment. This may become increasingly important as multinational firms continue to diversify production and supply chains under broader China Plus One strategies. Its long-term effectiveness, however, will depend on the government's ability to adapt regulatory practices to evolving technologies, changing supply-chain structures, and external policy developments. Decree 259 should therefore be viewed not as a final solution, but as an evolving framework whose success will be determined by how effectively security considerations are balanced with economic development and international integration.

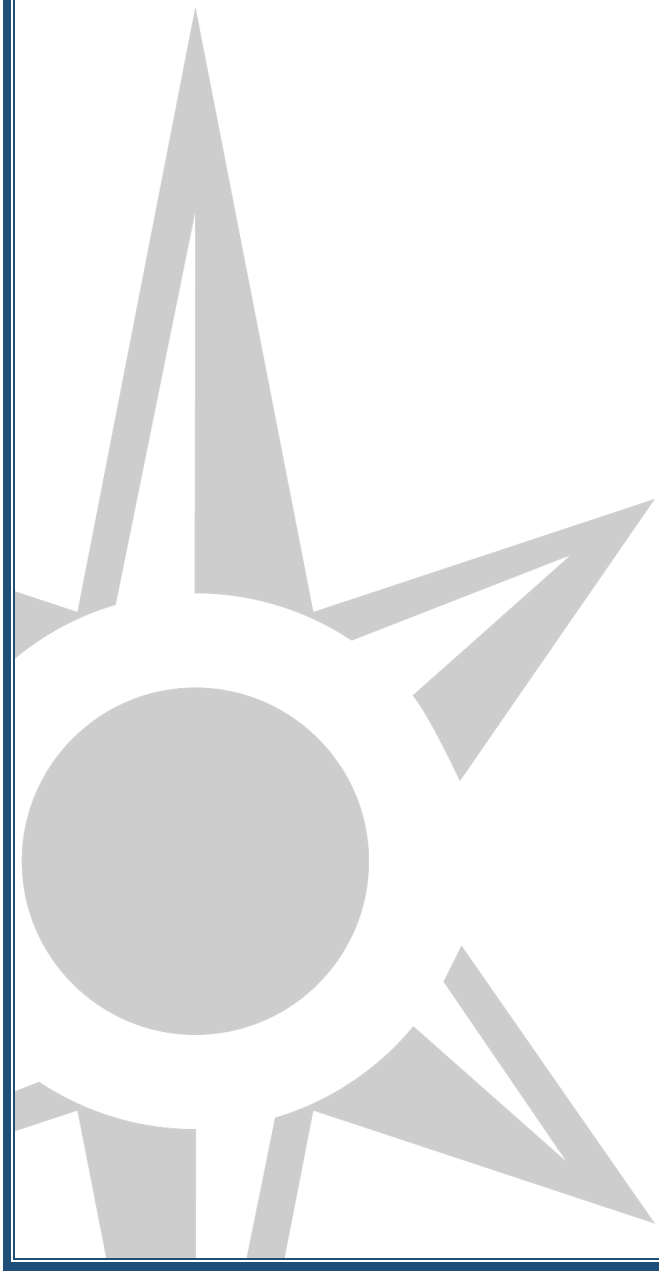
ABOUT THE AUTHOR

TRAN THI MONG TUYEN (Ms) is a PhD scholar at National Chengchi University, specializing in geopolitics, high technology, and Indo-Pacific regional affairs. She also contributes as a Guest Lecturer in Vietnam. She previously served as a Visiting Scholar at National Taiwan University and as a Non-Resident Handa Fellow at Pacific Forum. Earlier in her career, she was a Fellow at the European Union in Luxembourg. Since 2012, she has participated in the Young Leaders program at Pacific Forum. Ms. Tran has been invited to high-level Track 1.5 and Track 2 diplomacy conferences across the Indo-Pacific, including those organized by Council for Security Cooperation in the Asia-Pacific (CSCAP) and the Yushan Forum. She has also been a panelist at institutions such as Perry World House (US), IISS Asia (Singapore), and government-affiliated think tanks. Her academic research has been presented at leading university workshops worldwide. She has published in English, French, and Vietnamese in prominent magazines and journals. In addition, she frequently provides expert commentary for major international media outlets, including Nikkei Asia, The Diplomat, South China Morning Post, BBC News, Mainichi, and RTI, Taipei Times and among others, and has appeared in television interviews on networks such as Al-Qahera and Taiwan Plus. Her insights have been cited in six languages – Vietnamese, French, English, Chinese, Japanese, and Arabic, across international media in Asia. Ms. Tran earned a Master's degree in International Relations in the United Kingdom and also completed the Erasmus Mundus Master's program in France.

PACIFIC FORUM
INTERNATIONAL

Fortifying the Legal Framework for Semiconductor Layout Designs in Vietnam: Gaps and Policy Options under the National Semiconductor Strategy

By
Huong Tran



Executive Summary

Huong Tran

The global semiconductor industry is undergoing major changes. Many countries are trying to secure their supply chains and reduce dependence on the major players in the sector. These countries are investing more in a domestic capacity and are strengthening control over critical technologies. These shifts bring both opportunities and challenges for emerging economies like Vietnam. Vietnam is in a strategic position to participate in the global semiconductor value chain. The country has political stability and strong partnerships with major semiconductor powers. It also has a young, STEM-skilled workforce and reserves of rare earth materials. These advantages have attracted more than 50 semiconductor companies to Vietnam. Most of them focus on chip design, packaging, and testing. Some large multinational firms are also planning to expand their operations in the country.

In response, the Vietnamese government issued The National Strategy Decision. This decision approved the National Strategy for the Development of the Semiconductor Industry to 2030, with a vision to 2050. The strategy focuses on three main areas: training human resources, attracting investment, and improving the legal and institutional framework. In particular, it highlights the importance of intellectual property (IP) protection, export controls, and technology transfer.

Despite these developments, Vietnam still faces major legal and institutional challenges in protecting semiconductor- related IP. One key issue is the weak protection of layout designs, which are essential to the commercial value of chips. Over the last few years, Vietnam has begun joining international IP treaties and in 2025, revised their IP Law. Still, enforcement remains limited. Problems include weak intellectual property enforcement and unclear dispute resolution mechanisms. These issues can discourage innovation and reduce investor confidence due to fears of IP infringement and technology leakage.

This paper aims to assess the current legal and institutional gaps in protecting semiconductor- related IP in Vietnam. It will focus on layout designs. The goal is to develop practical legal and policy recommendations to help align Vietnam's IP system with international standards and support its national goals for semiconductor development.

Introduction

The global semiconductor industry is undergoing a period of profound restructuring driven by geopolitical tensions, supply chain vulnerabilities, and intensifying technological competition. In recent years, major economies have adopted policies aimed at reducing dependence on geographically concentrated production networks while strengthening domestic capabilities in critical technologies. These developments have elevated semiconductors from a purely economic sector to a strategic domain closely linked to national security, economic resilience, and technological sovereignty. As a result, participation in the semiconductor value chain increasingly depends not only on industrial capacity but also on the strength of legal and institutional frameworks, particularly in intellectual property protection.

Against this backdrop, emerging economies are seeking to position themselves within a rapidly evolving global landscape. Vietnam represents a particularly compelling case. The country combines political stability, expanding strategic partnerships with major semiconductor powers, and a growing pool of STEM-skilled labor. In addition, its integration into global trade agreements and access to critical raw materials enhance its attractiveness as a destination for semiconductor investment. These advantages have already led to a growing presence of multinational firms, with current activities concentrated in chip design, packaging, and testing. At the same time, the Vietnamese government has articulated ambitious goals through the National Strategy for the Development of the Semiconductor Industry to 2030, with a vision to 2050, which prioritizes human capital development, investment attraction, and institutional reform.

Despite this progress, the transition from a manufacturing-based to an innovation-driven semiconductor ecosystem requires more than industrial policy. It depends critically on the ability to protect high-value intangible assets. Among these, layout designs of semiconductor integrated circuits occupy a central role. Layout designs encapsulate the spatial configuration of circuits and represent a significant share of the technological and commercial value embedded in semiconductor products. Weak protection of such designs can expose firms to risks of imitation, reverse engineering, and misappropriation, thereby undermining incentives for innovation and limiting the potential for domestic capability upgrading.

While a substantial body of literature has examined semiconductor industrial policy, global value chains, and technology transfer in developing economies, relatively limited attention has been paid to the legal infrastructure underpinning these processes, particularly in the context of layout design protection. Existing studies on Vietnam have largely focused on investment trends, human capital development, and participation in lower value added segments of the semiconductor value chain. More broadly, the literature on intellectual property in emerging economies tends to emphasize patents, trademarks, and copyright, often overlooking the specific challenges associated with protecting layout designs—characterized by hybrid legal features and complex enforcement requirements. This creates a critical gap in understanding how legal and institutional frameworks can enable or constrain technological upgrading in the semiconductor sector.

This paper addresses this gap by examining the protection of layout designs of semiconductor integrated circuits in Vietnam from a legal and policy perspective. It advances the argument that, despite recent reforms and international commitments, Vietnam's current framework remains insufficient to support its ambitions of moving up the semiconductor value chain and achieving high-income status. In particular, weaknesses in legal clarity, enforcement capacity, and dispute resolution mechanisms continue to pose significant barriers to effective protection.

The contribution of this study is threefold. First, it provides a systematic assessment of Vietnam's existing legal and institutional framework for protecting semiconductor-related intellectual property, with a focus on layout-designs. Second, it identifies key gaps and constraints in both substantive law and enforcement practices, situating these within the broader context of global semiconductor governance. Third, it develops targeted legal and policy recommendations aimed at strengthening protection mechanisms, enhancing regulatory coherence, and improving investor confidence. By doing so, the paper contributes to both the academic literature on intellectual property and development and to ongoing policy debates on how emerging economies can leverage legal frameworks

to support participation in high-technology industries.

Ultimately, the study argues that strengthening the protection of layout designs is not merely a technical legal reform but a strategic policy imperative. It is essential for fostering innovation, attracting high-quality investment, and enabling Vietnam to transition toward a resilient, innovation-driven, and high-income economy.

Why This is Critical

The strengthening of legal protection for layout designs of semiconductor integrated circuits is not a peripheral legal issue; rather, it is a central policy concern for Vietnam's long-term economic transformation. It sits at the intersection of industrial strategy, innovation policy, and global economic integration. This section advances three interrelated arguments to explain why this issue is critical: (i) the importance of semiconductors as a strategic industry for Vietnam's high-income ambition; (ii) the constraints imposed by weak protection on industrial upgrading; and (iii) the urgency of addressing legal gaps to unlock sustainable growth within the global semiconductor value chain.

First, semiconductors have been explicitly identified by the Vietnamese government as a strategic industry under Decision No. 1018/QĐ-TTg, reflecting their foundational role in modern economies.

Overview of Vietnam's National Semiconductor Strategy (Decision No. 1018/QĐ-TTg).

Vietnam's National Strategy for the Development of the Semiconductor Industry to 2030, with a vision to 2050 (Decision No. 1018/QĐ-TTg), provides a comprehensive roadmap for positioning the country within the global semiconductor value chain. The strategy reflects a long-term ambition to transform Vietnam from a participant in lower value added segments into a competitive hub for semiconductor innovation, production, and integration.

At the core of the strategy is a development framework summarized by the formula **"C = SET + 1"**, which captures the structural components of Vietnam's semiconductor ecosystem. In this formulation, C (Chip) represents the ultimate objective of developing a domestic semiconductor industry, while S (Specialized) emphasizes the strategic focus on specialized chips tailored to key sectors such as artificial intelligence and the Internet of Things. E (Electronics) highlights the close integration between the semiconductor and electronics industries, recognizing that downstream electronics manufacturing provides both demand and scale for semiconductor development. T (Talent) underscores the central role of human capital, particularly in engineering and design capabilities. **The "+1"** component positions Vietnam itself as a safe and emerging destination within global semiconductor supply chains, leveraging its geopolitical positioning and economic openness.

The strategy is implemented through a three-phase roadmap to 2050, reflecting a gradual upgrading trajectory. In the first phase (2024–2030), Vietnam aims to leverage its geopolitical advantages and human resources to attract selective foreign direct investment (FDI) while building foundational capabilities across the semiconductor value chain, including in research, design, fabrication, packaging, and testing. This phase prioritizes the development of at least 100 design firms, the establishment of initial fabrication capacity, and the expansion of packaging and testing facilities along with a workforce target of over 50,000 skilled engineers.

In the second phase (2030–2040), the strategy envisions Vietnam becoming a global center for semiconductor and electronics industries, combining domestic capacity with continued FDI inflows. This stage focuses on scaling up design capabilities, increasing fabrication capacity, and moving toward partial technological self-reliance, with the number of design firms expected to double and industry revenues anticipated at over USD 50 billion annually.

The third phase (2040–2050) aims to position Vietnam among the leading countries in the global semiconductor industry, with full mastery of research and development capabilities and a mature, self-reliant ecosystem. By 2050, the semiconductor industry is projected to generate over USD 100 billion in annual revenue, with significantly higher domestic value added and a fully developed industrial ecosystem capable of leading in selected segments of the value chain.

To achieve these objectives, the strategy identifies five key policy pillars. First, it prioritizes the development of specialized semiconductor products through investment in core technologies, research

centers, and shared infrastructure, as well as mechanisms such as multi-project wafer (MPW) production to support innovation and reduce costs. Second, it promotes the expansion of the electronics industry as a complementary sector, creating demand for semiconductor products and fostering industrial linkages. Third, it emphasizes human capital development through large-scale training programs, international cooperation, and policies to attract global talent. Fourth, it outlines an ambitious framework for attracting high-quality FDI, including preferential policies, infrastructure development, and mechanisms to mitigate the impact of global minimum tax rules. Finally, it includes cross-cutting measures such as institutional coordination, standard-setting, financial support for research and development, international cooperation, and environmental sustainability.

Importantly, while Decision 1018 focuses primarily on industrial and investment policy, its successful implementation also depends on the strength of the underlying legal and institutional framework. As the strategy places increasing emphasis on higher value added segments - especially chip design and innovation - the effective protection of intangible assets, including layout designs, is increasingly important for creating incentives for investment and innovation and, untimately, for achieving the strategy's objectives. In this sense, the strategy not only outlines an industrial vision but also highlights the need for complementary legal reforms to ensure that Vietnam can fully realize its ambitions within the global semiconductor ecosystem.

Beyond their economic value, semiconductors underpin a wide range of critical sectors, including telecommunications, artificial intelligence, defense technologies, and digital infrastructure. For Vietnam, the development of a competitive semiconductor industry is closely linked to its broader objective of transitioning from a manufacturing-based economy to an innovation-driven, high-income economy. Such a transition requires a structural shift away from labor-intensive production and toward knowledge-intensive activities, where value is increasingly derived from intangible assets, technological capabilities, and proprietary knowledge.

Within this context, the semiconductor value chain is inherently intellectual property-intensive. While downstream activities such as assembly, packaging, and testing contribute to employment and export revenues, the highest value-added segments are concentrated in design and advanced manufacturing, where intellectual property plays a decisive role. Among the various forms of IP, layout designs of semiconductor integrated circuits are particularly significant. These designs capture the spatial configuration of electronic circuits and embody complex engineering solutions that are costly and time-consuming to develop. As such, they represent core assets at the design stage and form a critical foundation for a functioning innovation ecosystem. Effective protection of layout designs is therefore essential—not only for safeguarding individual firms' investments but also for enabling cumulative innovation, knowledge diffusion under controlled conditions, and the development of domestic design capabilities.

Second, the absence of strong and reliable protection for layout designs imposes structural constraints on Vietnam's ability to move up the semiconductor value chain. At present, most semiconductor-related activities in Vietnam remain concentrated in lower value added segments, particularly assembly and testing. While these segments provide important entry points into global production networks, they offer limited opportunities for technological learning and value capture compared to design-intensive activities. Weak protection exacerbates this situation by increasing the risks associated with investing in higher value-added functions. Insufficient safeguards against unauthorized copying, reverse engineering, and misappropriation of layout designs, in particular, reduce the incentives for both domestic firms and foreign investors to engage in advanced design activities within Vietnam.

From the perspective of multinational enterprises, decisions regarding the location of research and development (R&D) and design functions are highly sensitive to the strength of local IP regimes. Firms are unlikely to transfer core technologies or establish high-value operations in jurisdictions where legal protection is uncertain or enforcement is ineffective. As a result, weak protection can limit the quality of foreign direct investment (FDI), confining Vietnam to a role within the lower tiers of the value chain. For domestic firms, the absence of robust protection mechanisms undermines the returns to innovation, discouraging investment in design capabilities and reducing the likelihood of indigenous technological development. In this sense, the protection of layout designs is not merely a legal safeguard but a

prerequisite for industrial upgrading and meaningful participation in higher value-added segments of the semiconductor industry.

Third, addressing existing legal and institutional gaps is essential to unlocking Vietnam's strategic growth potential in the semiconductor sector. Despite recent efforts to align its intellectual property framework with international standards, important shortcomings remain in both substantive law and enforcement. These include ambiguities in the scope of protection, procedural inefficiencies, and limited capacity for resolving complex, technology-related disputes. Such gaps create uncertainty for rights holders and weaken the overall credibility of the legal system. In a sector where innovation cycles are rapid and competitive pressures are intense, even modest levels of uncertainty can have disproportionate effects on investment decisions.

If these issues are not addressed in a timely manner, Vietnam risks missing a critical window of opportunity to integrate more deeply into the global semiconductor value chain. The current phase of industry restructuring has created openings for new entrants, but these opportunities are contingent on the ability to provide a secure and predictable legal environment. Without targeted legal reforms, Vietnam may remain locked into lower value added activities, unable to capture the full benefits of its strategic positioning and policy ambitions. Conversely, strengthening the protection of layout designs through clearer legal provisions, more effective enforcement, and credible dispute resolution mechanisms can serve as a catalyst for attracting high-quality investment, fostering domestic innovation, and enhancing Vietnam's role within global production networks.

It must be stressed that these three dimensions underscore the critical importance of layout design protection in Vietnam's development trajectory. It is not simply a matter of compliance with international norms but a strategic instrument for enabling industrial upgrading, supporting innovation, and advancing the country's transition toward a high-income, knowledge-based economy.

Legal Framework for Layout Design Protection

While Decision No. 1018/QĐ-TTg is primarily framed as an industrial and development strategy, its effective implementation is inherently contingent upon the robustness of Vietnam's legal and institutional framework. Specifically, as the strategy seeks to reposition Vietnam toward higher value added segments of the semiconductor value chain, the role of law—especially in governing intellectual property, technology transfer, and dispute resolution—becomes increasingly central rather than merely supportive.

The transition envisioned under the strategy from assembly and test toward design, fabrication, and innovation implies a structural shift in the nature of value creation. In lower segments of the value chain, competitive advantage is largely derived from cost efficiency and labor availability. This shift necessarily places greater demands on the legal system to provide clear, predictable, and enforceable rules governing the ownership, use, and transfer of such assets.

Within this context, intellectual property protection assumes a foundational role. The strategy's emphasis on developing domestic design capabilities, promoting specialized semiconductor products, and fostering R&D activities implicitly requires a legal environment in which innovation can be effectively protected and commercially exploited. Among the various forms of intellectual property, the protection of layout designs of semiconductor integrated circuits is of particular importance.

Beyond substantive IP protection, the broader institutional environment also plays a decisive role. Effective enforcement mechanisms, including administrative, civil, and judicial remedies, are essential to ensure that legal rights are not merely formal but practically meaningful. Similarly, the availability of efficient and credible dispute resolution mechanisms—whether through courts or alternative forums such as arbitration and mediation - directly affects the level of confidence among both domestic and foreign investors. In technology-intensive sectors such as semiconductors, where disputes often involve complex technical and commercial issues, delays or inconsistencies in enforcement can have significant economic consequences.

The strategy's strong emphasis on attracting high-quality foreign direct investment further reinforces the importance of legal certainty. Multinational enterprises typically assess not only economic incentives but also the reliability of the host country's

legal framework when making investment decisions, particularly with respect to R&D activities and the localization of core technologies. A legal system that ensures effective protection of intellectual property, facilitates secure technology transfer, and provides predictable dispute resolution mechanisms is therefore a critical determinant of Vietnam's ability to attract and retain such investment.

At the same time, the strategy highlights the need for greater institutional coordination and regulatory coherence. The development of a semiconductor ecosystem involves multiple regulatory domains, including investment law, intellectual property law, competition law, and sector-specific regulations. Fragmentation or inconsistency across these areas can create legal uncertainty and increase compliance costs for firms. Accordingly, strengthening institutional capacity and ensuring alignment across relevant legal frameworks are essential components of the broader reform agenda implied by Decision 1018.

In this respect, the strategy may be understood not only as an industrial policy document but also as a catalyst for legal and institutional modernization. Its successful implementation depends on the extent to which Vietnam can develop a legal framework able to support innovation, protecting high-value intangible assets, and facilitating integration into global technology networks. Without such a framework, the country risks remaining confined to lower value-added segments of the semiconductor value chain, despite its strategic ambitions and favorable structural conditions.

In sum, strengthening the protection of intellectual property—particularly layout designs—enhancing enforcement mechanisms, and improving dispute resolution systems are essential steps in translating the strategy's vision into tangible outcomes. These reforms will play a decisive role in determining whether Vietnam can successfully advance toward a more innovation-driven, resilient, and high-value semiconductor industry.

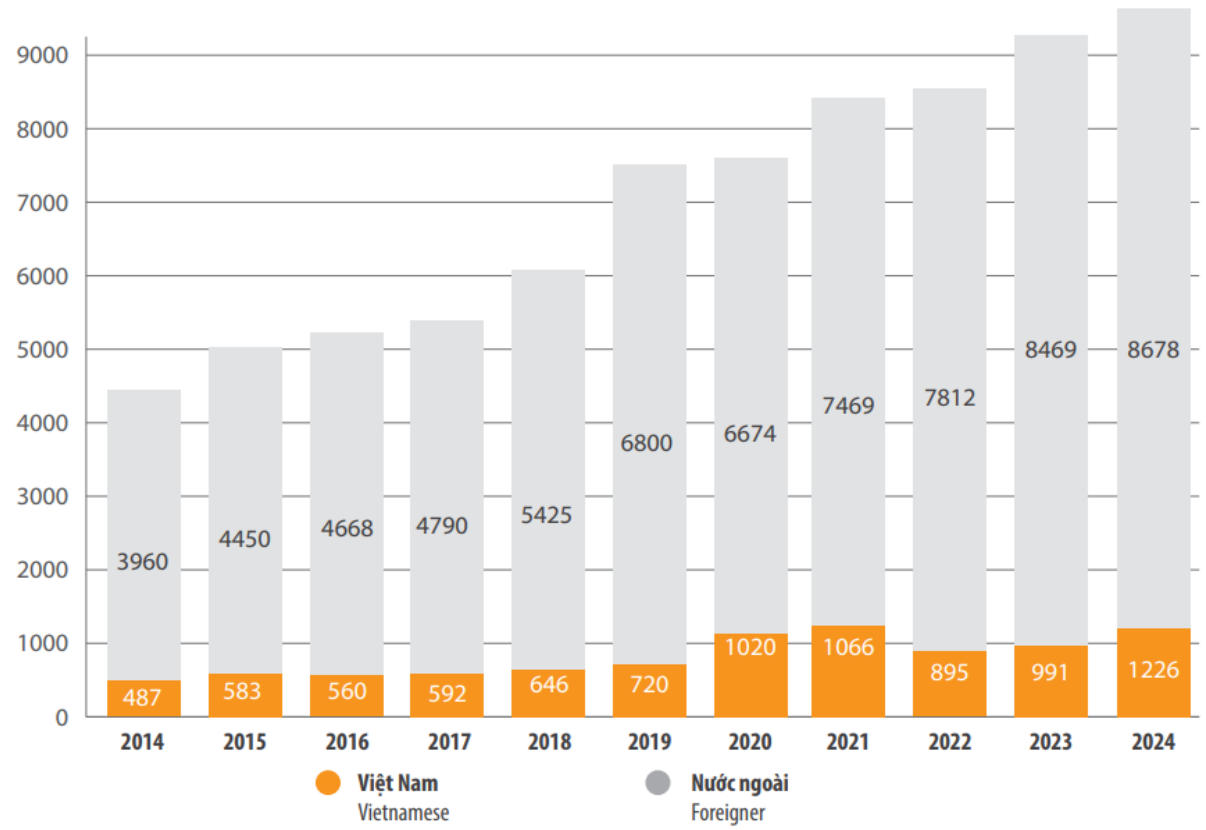
Vietnam operates within a dual legal framework encompassing both international obligations and domestic legislation—most notably the Agreement on Trade-Related Aspects of Intellectual Property Rights (TRIPS). Vietnam has effectively internalized these international standards into its national legal system, ensuring compliance with global norms.

At the domestic level, the 2025 Law on Intellectual Property, now in its fourth iteration of amendments and accompanied by implementing regulations, consolidates all categories of intellectual property rights within a single statute. While most jurisdictions maintain separate legal instruments for different types of IP, Vietnam's unified approach reflects its legislative evolution over the past two decades and aligns with the nation's broader economic trajectory—from a low-income economy to a middle-income country with the ultimate aspiration of high-income status by 2045. Notably, the volume of trademark applications expanded from approximately 10,000 in 2005 to over 70,000 in 2025, illustrating the dramatic growth in IP activity and the concomitant need for a responsive legal framework.

NUMBER OF INDUSTRIAL PROPERTY REGISTRATION APPLICATIONS RECEIVED, PROCESSED AND ISSUED IN 2024 (COMPARED TO 2023)

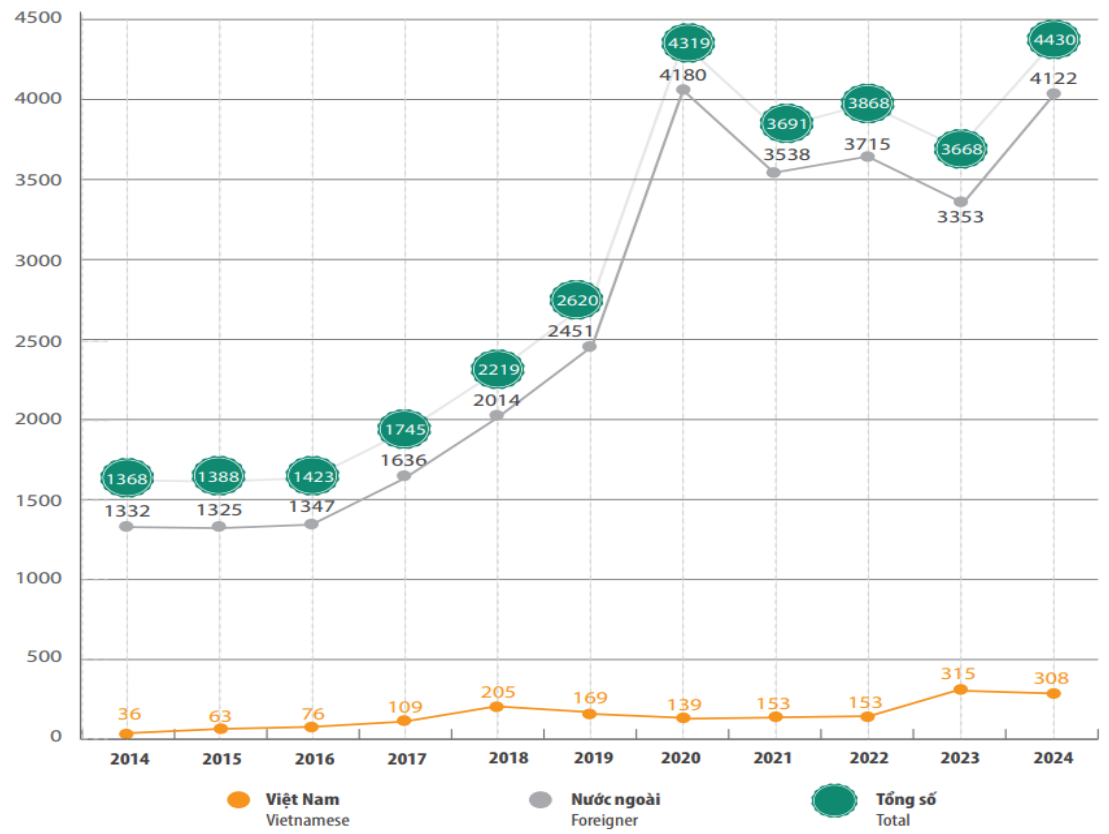
No.	Type of application	Number of applications received			Number of applications processed (Denied + accepted)			Number of protections granted		
		2023	2024	Compare	2023	2024	Compare	2023	2024	Compare
1	Inventions, utility solutions	10295	10796	4.9%	8451	9581	13.4%	4136	4875	17.9%
1.1	Inventions	9460	9904	4.7%	7835	8987	14.7%	3668	4430	20.8%
1.2	Utility solutions	835	892	6.8%	616	594	-3.6%	468	445	-4.9%
2	Industrial Designs	3738	3796	1.6%	3104	3311	6.7%	1852	2001	8.0%
2.1	National applications	3210	3222	0.4%	3092	2648	-14.4%	1852	2001	8.0%
2.2	International applications (submitted under The Hague System)	528	574	8.7%	12	663	5425.0%	-	-	
3	Trademarks	70370	74072	5.3%	62239	73813	18.6%	30983	46787	51.0%

No.	Type of application	Number of applications received			Number of applications processed (Denied + accepted)			Number of protections granted		
		2023	2024	Compare	2023	2024	Compare	2023	2024	Compare
3.1	National applications	60929	64112	5.2%	52968	64312	21.4%	30983	46787	51.0%
3.2	International application (submitted under the Madrid System)	9441	9960	5.5%	9271	9501	2.5%	-	-	
4	Geographical Indications	14	23	64.3%	7	9	28.6%	6	11	83.3%
5	International application of Vietnamese origin	336	346	3.0%	329	334	1.5%		-	
5.1	Inventions	12	16	33.3%	12	16	33.3%	-	-	
5.2	Trademarks	323	330	2.2%	316	318	0.6%	-	-	
5.3	Industrial designs	1	-		1	-		-	-	
Total		84,753	89,033	5.0%	74,130	87,048	17.4%	36,977	53,674	45.2%



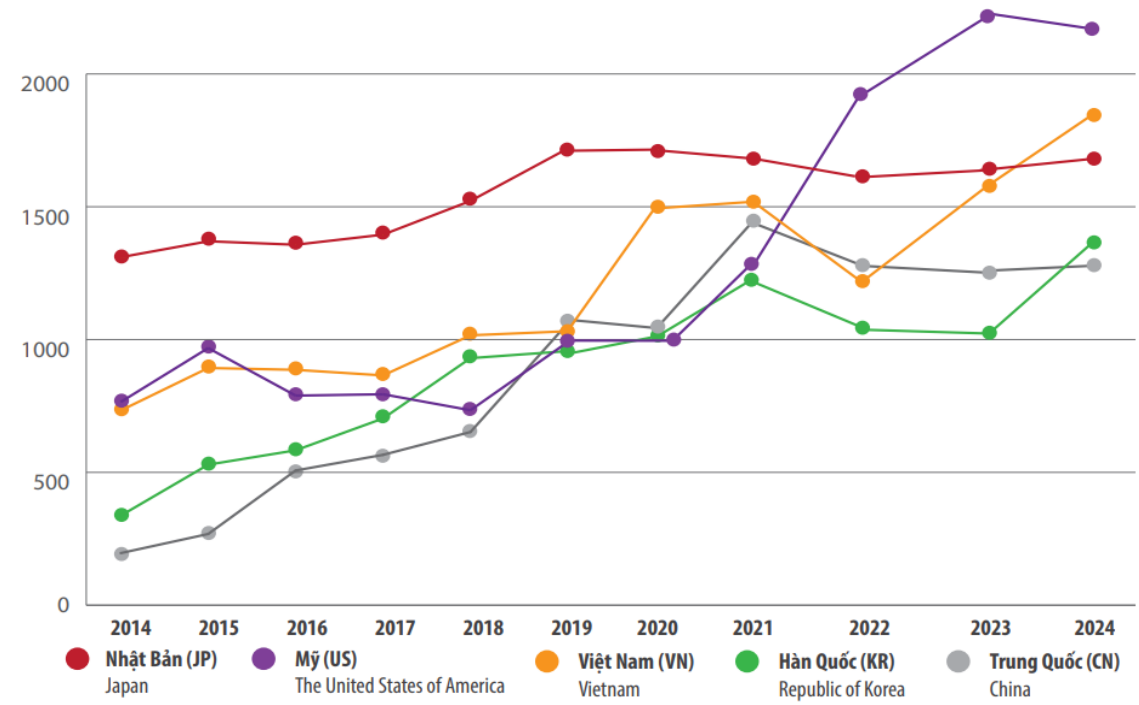
Số lượng đơn đăng ký sáng chế từ năm 2014 đến 2024 của chủ đơn Việt Nam và nước ngoài

Invention applications filed from 2014 to 2024 by the Vietnamese and the Foreigner



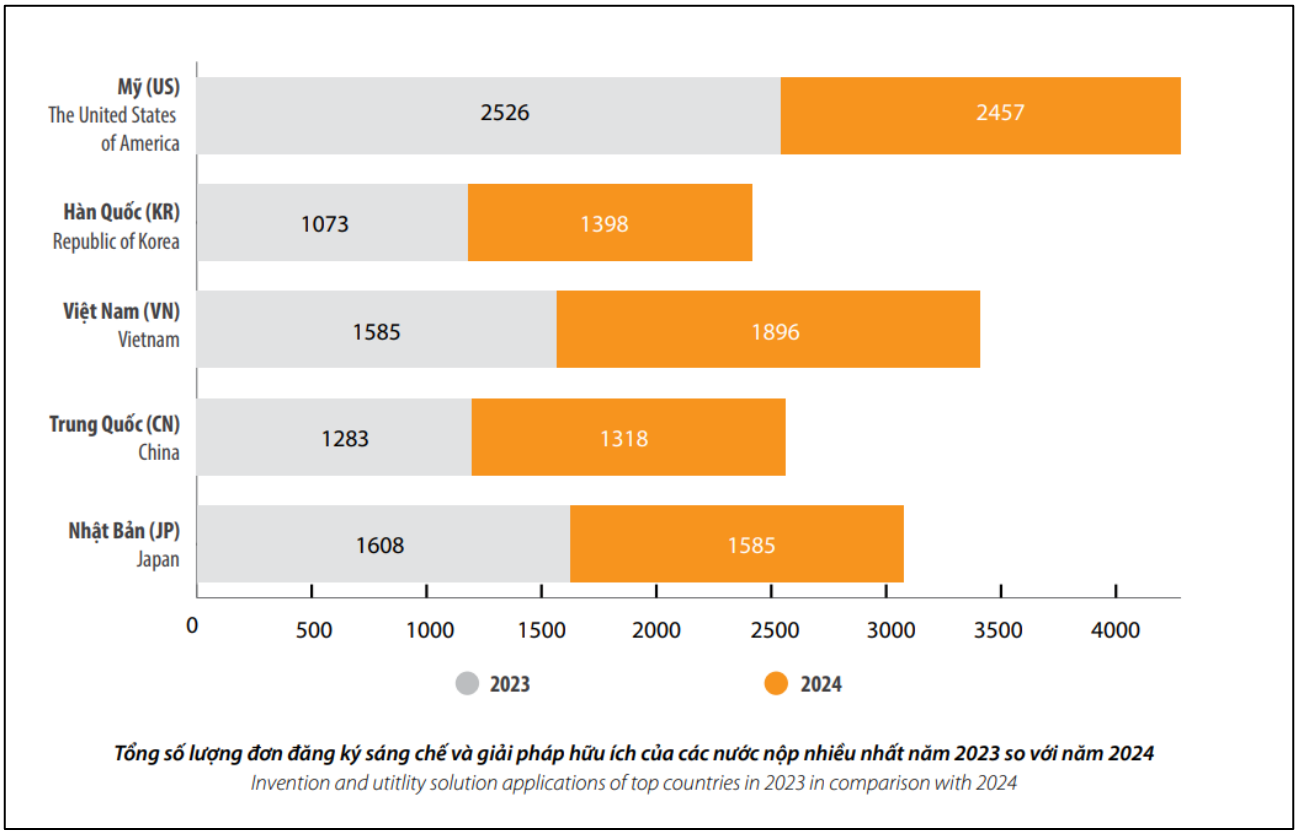
Số lượng bằng độc quyền sáng chế đã cấp từ năm 2014 đến 2024 của chủ đơn Việt Nam và nước ngoài

Invention patents granted from 2014 to 2024 by the Vietnamese and the Foreigner



Sự gia tăng tổng số lượng đơn đăng ký sáng chế và giải pháp hữu ích của các nước có đơn nộp nhiều nhất trong giai đoạn 2014 đến 2024

The increase in invention and utility solution applications of top countries during 2014 -2024



Source: VNIPO: ANNUAL REPORT OF INTELLECTUAL PROPERTY OF VIETNAM 2024

Beyond the primary IP statute, Vietnam has developed a suite of related legal instruments to govern enforcement and dispute resolution, including the Civil Procedure Code, the Law on Commercial Arbitration, and Decree No. 22 on commercial mediation. Investors in the semiconductor sector must also navigate a broader legal ecosystem encompassing investment, land use, labor, taxation, high technology, and innovation laws.

Layout designs of semiconductor integrated circuits represent a particularly specialized category of IP. Filing volumes are minimal relative to other IP forms and are often omitted from statistical reports. Nonetheless, layout design rights intersect with other forms of IP, forming a "bundle of rights" that may include copyrights and trade secrets. The technical complexity of semiconductor designs, combined with the layered legal framework, generates gaps in both enforcement and litigation which are likely to intensify as Vietnam prioritizes innovation and IP commercialization.

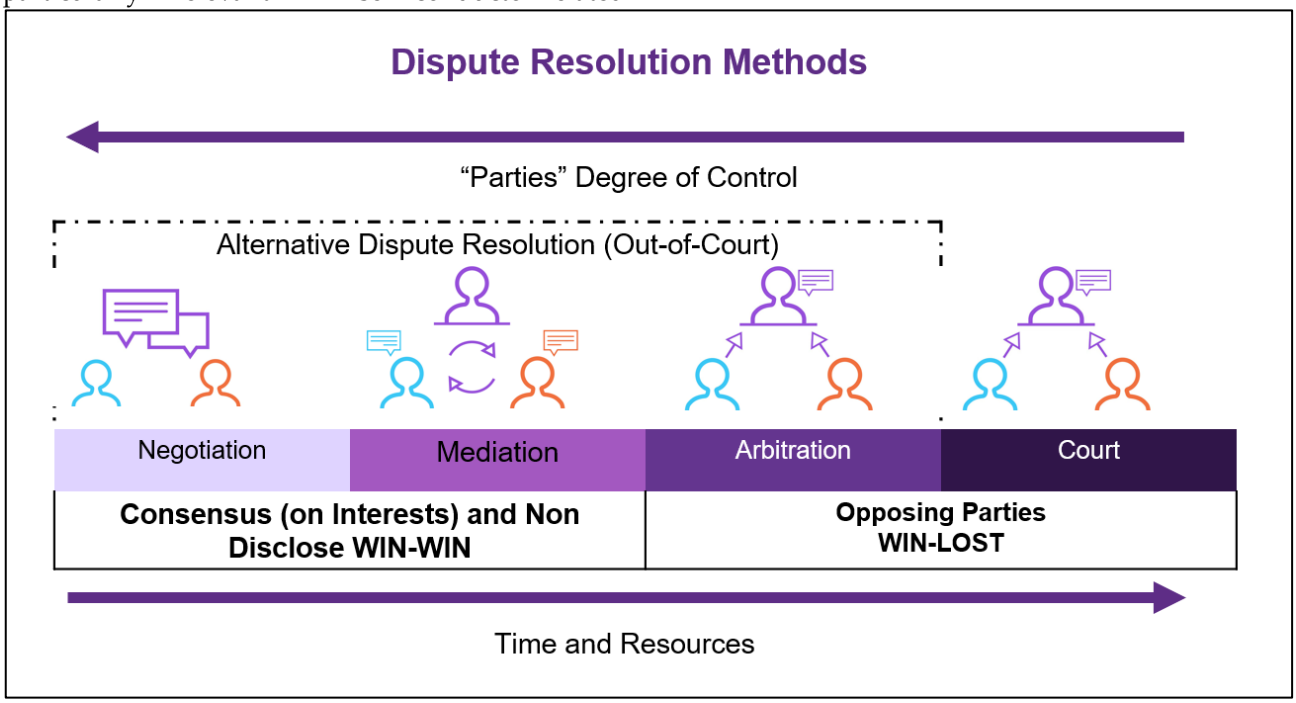
Currently, administrative measures are the most frequently utilized enforcement tools due to the authority granted to regulatory agencies; however, judicial enforcement remains protracted, often spanning three to five years through multiple levels of adjudication, including first-instance trials, appeals, and occasional remands. This duration can incentivize misuse of administrative measures for anti-competitive purposes. International best practice encourages civil remedies as a primary mechanism for resolving IP disputes, supported by alternative dispute resolution (ADR) methods such as mediation and arbitration. ADR is particularly suitable for IP disputes, as it preserves confidentiality, promotes sustainable commercial relationships, and aligns with investor expectations regarding the rule of law - a key determinant of foreign investment. Current assessments indicate that Vietnam ranks below regional and global averages on this metric, underscoring the urgency of legal and procedural reform.

The table below shows that dispute resolution mechanisms play a critical role in the effective enforcement of intellectual property rights, particularly in highly technical sectors such as semiconductors. In Vietnam, the legal framework provides for multiple avenues of dispute resolution, including litigation before courts, commercial arbitration, mediation, and administrative enforcement. Each of these mechanisms is grounded in distinct legal instruments, such as the Civil

Procedure Code, the Law on Commercial Arbitration, and other relevant regulations on commercial mediation. Each reflects different policy objectives and institutional capacities. Litigation remains the primary formal mechanism, offering binding and enforceable judgments backed by state authority. In practice, however, judicial proceedings in IP disputes are often protracted, frequently extending over several years due to multi-tiered adjudication processes. This delay not only undermines the timely protection of rights but also reduces the overall effectiveness of judicial remedies, particularly in fast-moving technology sectors where commercial value may dissipate rapidly.

In contrast, alternative dispute resolution (ADR) mechanisms, including arbitration and mediation, provide greater flexibility, confidentiality, and efficiency. Arbitration allows parties to select specialized adjudicators with technical expertise, while mediation facilitates mutually beneficial outcomes that preserve commercial relationships and protect sensitive information. These features are particularly relevant in semiconductor-related disputes, where proprietary knowledge, trade secrets, and layout designs are often at stake. Despite these advantages, the use of ADR in Vietnam remains relatively limited, partly due to entrenched legal culture and the lack of institutional capacity and awareness among stakeholders.

Administrative enforcement constitutes another distinctive feature of Vietnam's intellectual property regime. Authorities are empowered to impose sanctions and address infringements in a relatively swift and cost-effective manner. As a result, administrative measures have become the most commonly used enforcement tool in practice. However, this reliance raises important policy concerns. Administrative actions may not fully resolve underlying disputes, and in some cases, they may be strategically employed by parties as instruments of unfair competition. This divergence from international best practices - where civil remedies are typically prioritized - suggests the need for recalibration.



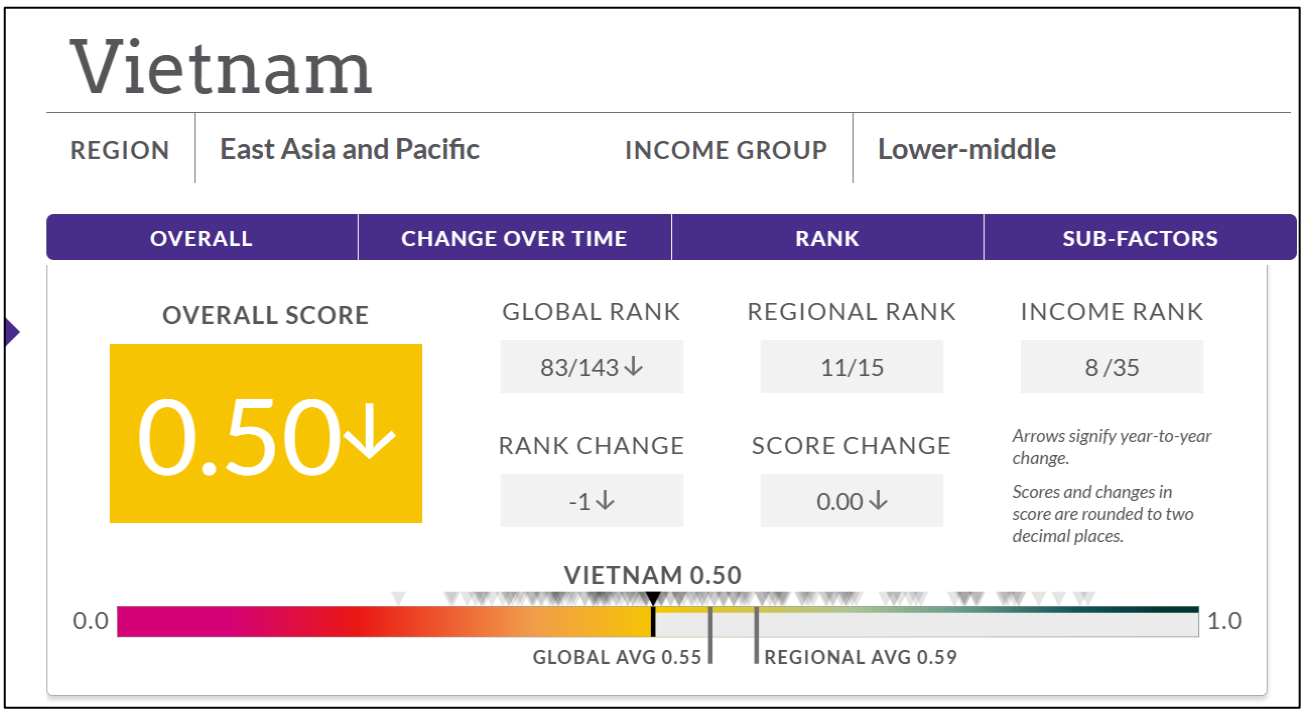
From a policy perspective, the current distribution of dispute resolution mechanisms reveals a structural imbalance. While administrative enforcement provides short-term efficiency, it does not substitute for a robust and credible judicial system capable of handling complex intellectual property disputes. Strengthening judicial capacity, reducing procedural delays, and enhancing technical expertise within courts are therefore essential reforms. At the same time, promoting ADR mechanisms should be a strategic priority, particularly in sectors characterized by rapid innovation and high levels of technical complexity. Encouraging the use of mediation and arbitration through legal incentives, institutional development, and capacity-building initiatives would align Vietnam more closely with international standards and improve investor confidence.

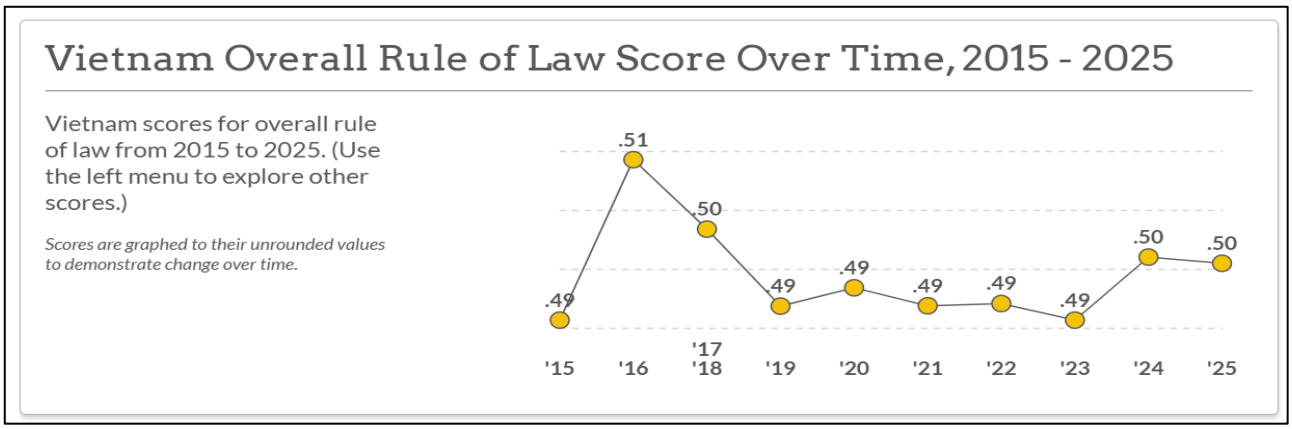
Ultimately, an effective dispute resolution framework must balance efficiency, fairness, and legal certainty.

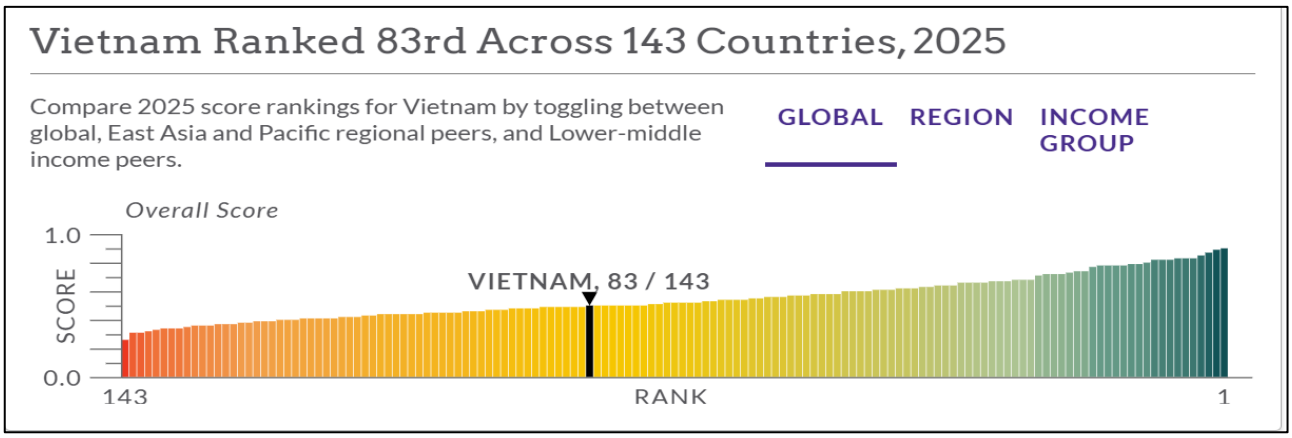
RESOLUTION OF CONTRACT DISPUTES IN VIETNAM (Doing Business Report 2014-2019)

Indicator	Vietnam
Time (days)	**400**
Filing and service	50
Trial and judgment	200
Enforcement of judgment	150
Cost (% of claim value)	**29.0**
Attorney fees (% of claim value)	21.0
Court fees (% of claim value)	5.0
Enforcement fees (% of claim value)	3.0
Quality of judicial processes	**6.5**
Court structure and proceedings	3.0
Case management	**1.0**
Court automation	0
Alternative dispute resolution (ADR)	2

This table demonstrates that dispute settlement under court procedures has been recognized as being time-and-cost consuming in Vietnam. The World Bank's annual Doing Business Reports from 2004-2020 show that the duration for contractual dispute settlement in the first-instance court of Viet Nam is 400 days or more (including approximately 250 days for case settlement at court and 150 days of judgment enforcement) and the dispute settlement cost accounts for 29% of the value of the case. On average, about 2.5% to 3% of the total number of cases handled by the tribunal system annually are overdue. Moreover, unofficial expenses in court settlement have tended to increase. Regarding dispute settlement by arbitration, statistics of Vietnam International Commercial Arbitration Center (VIAC) show that the average time for resolving a dispute is 153 days. This practice pushes businesses to seek other dispute settlement methods, including illegal ones.







Rule of law index (-2.5 weak; 2.5 strong), 2024: The average for 2024 based on 11 countries was -0.24 points. The highest value was in Singapore: 1.43 points and the lowest value was in Burma (Myanmar): -1.81 points. The indicator is available from 1996 to 2024. Below is a chart for all countries where data are available.

Measure: points; Source: The World Bank

South East | Download data from our database

Countries	Rule of law, 2024	Global rank	Available data
Singapore	1.43	1	1996 - 2024
Brunei	0.59	2	1996 - 2024
Malaysia	0.35	3	1996 - 2024
India	-0.04	4	1996 - 2024
Indonesia	-0.21	5	1996 - 2024
Thailand	-0.22	6	1996 - 2024
Vietnam	-0.31	7	1996 - 2024
Philippines	-0.57	8	1996 - 2024
Laos	-0.74	9	1996 - 2024
Cambodia	-1.06	10	1996 - 2024
Burma	-1.81	11	1996 - 2024

The figure above indicates that Vietnam's Rule of Law index remains relatively low, with an overall score of approximately 0.50, falling below both the global average (0.55) and the regional average in East Asia and the Pacific (0.59). In global terms, Vietnam ranks 83rd out of 143 countries, reflecting the infancy

in Rule of Law adoption. More concerning, however, is Vietnam's relative position within its immediate neighborhood. Within Southeast Asia, Vietnam's performance is comparatively weak: among 11 countries in the region, its rule of law score is higher only than that of the Philippines, Laos, Cambodia, and Myanmar, placing it in the lower tier of regional rankings. This suggests that Vietnam is not only under performing against global benchmarks but is also lagging many of its direct regional competitors.

From a policy perspective, this relatively low level of rule of law has significant implications for the country's investment climate. The Rule of Law index captures key dimensions such as legal certainty, effectiveness of contract enforcement, protection of property rights, and the quality of judicial processes. Weaknesses in these areas tend to increase regulatory uncertainty and transaction costs while reducing the predictability that investors require for long-term planning.

Vietnam's relatively low ranking within Southeast Asia is particularly problematic because investors often make comparative decisions within the region. Countries with stronger rule of law frameworks are perceived as offering more reliable dispute resolution mechanisms, better protection against expropriation or unfair competition, and a more transparent regulatory environment. As a result, Vietnam risks being at a competitive disadvantage in attracting high-quality foreign direct investment, especially in sectors that require robust legal safeguards and long-term commitments.

Moreover, the stagnation of Vietnam's Rule of Law score over time suggests that improvements in legal and institutional quality have not kept pace with the country's economic ambitions. This disconnect may undermine broader policy objectives, including efforts to move up the global value chain and to develop a competitive semiconductor industry. Strengthening judicial capacity, enhancing enforcement mechanisms, and promoting alternative dispute resolution methods are therefore not merely legal reforms but essential components of a broader strategy to improve investor confidence. Without substantive progress in these areas, Vietnam may face increasing difficulty in positioning itself as a credible and attractive destination for technology-driven investment in an increasingly competitive regional landscape.

Recommendations

A robust legal and regulatory framework is foundational to fostering a resilient and globally competitive semiconductor ecosystem in Vietnam. Building on the analyses above which highlight Vietnam's rapid growth potential in semiconductor manufacturing, the strategic importance of semiconductors for national security, and existing gaps in intellectual property (IP) and investment frameworks - this section outlines an integrated set of policy recommendations. These recommendations aim to reinforce the rule of law, protect domestic innovation, and enhance investor confidence in high-tech sectors, particularly semiconductors. They are aligned with the objectives of Decision No. 1018/QĐ-TTg, which emphasizes industrial resilience, technological self-reliance, and integration into global supply chains.

1. Strengthening the Rule of Law to Attract Investment

A predictable and transparent legal environment is critical for attracting both domestic and foreign investment in high-technology sectors. Strengthening the rule of law should prioritize the enforcement of intellectual property rights and investment laws, as these are key determinants of investor confidence. Analysis indicates that uncertainty in IP enforcement, slow judicial procedures, and inconsistent application of regulations can deter foreign investors and constrain domestic firms from engaging in high-risk, high-value semiconductor innovation.

Policy measures should include enhancing judicial efficiency and transparency through targeted reforms, such as specialized IP benches in commercial courts, clear procedural guidelines for patent and industrial design enforcement, and systematic reporting on case outcomes. Aligning Vietnam's legal and regulatory framework with international best practices- including WIPO standards and frameworks observed in major semiconductor-producing economies - will facilitate foreign investment and ensure that domestic firms are prepared to compete in global supply chains. Such alignment also underscores Vietnam's commitment to upholding the rule of law, creating a predictable environment that is essential for long-term industrial growth.

2. Enactment of a Dedicated Law on Layout-Designs

A central policy priority is the passage of a dedicated law protecting layout designs of semiconductor integrated circuits. Currently, the absence of a specialized legal framework creates uncertainty for innovators and investors, discouraging R&D and limiting domestic participation in global value chains. A dedicated law would clearly define the scope of rights, establish precise criteria for infringement, and provide effective enforcement mechanisms, thereby incentivizing domestic innovation and technology transfer.

The legislation should adopt internationally recognized standards to ensure compatibility with global practices and facilitate cross-border protection of intellectual property. It should also integrate enforcement mechanisms with existing IP and commercial courts, as well as alternative dispute resolution bodies, to ensure timely and effective protection of rights. By providing legal certainty, this law would support Vietnamese firms in leveraging government incentives under Decision No. 1018/QĐ-TTg, including preferential investment treatment for semiconductor manufacturing and R&D activities. This would further enhance Vietnam's attractiveness as a destination for high-tech investment while reinforcing domestic capabilities in semiconductor design and production.

Given these dynamics, enacting dedicated legislation for layout designs is both urgent and strategically necessary. Such legislation must account for unique legal, technical, and commercial complexities, including standards for technological disclosure, trade secrets protection, and harmonization with broader IP and semiconductor policy. Recognizing the extended legislative timeline in Vietnam - typically 7–10 years from draft to enactment prioritization within the next one to two years is essential to ensure alignment with the National Semiconductor Strategy and to mobilize the necessary technical and legal resources.

3. Support for Alternative Dispute Resolution: Arbitration and Mediation

Finally, efficient resolution of IP and commercial disputes is essential to maintain investor confidence and foster innovation. While judicial reforms are ongoing, promoting ADR mechanisms - offers a complementary pathway to resolve disputes efficiently, reduce costs, and provide predictability.

To operationalize this recommendation, Vietnam should establish specialized IP arbitration panels or high-tech dispute centers staffed with technical and legal experts. These institutions should operate under internationally recognized rules, providing parties with confidence in impartiality and enforceability. Additionally, incentivizing mediation for early-stage conflicts can prevent protracted litigation, preserve commercial relationships, and encourage compliance with contractual and IP obligations. By integrating ADR into the broader legal ecosystem, Vietnam can provide a flexible, investor-friendly dispute resolution framework that enables parties to resolve conflicts efficiently while reducing the costs, uncertainty, and disruption associated with prolonged litigation.

Promoting ADR mechanisms should remain a central policy objective. ADR has demonstrated effectiveness in developed jurisdictions worldwide, and Vietnam cannot afford to lag behind. Integrating ADR into IP enforcement will enhance legal certainty, foster investor confidence, and support the nation's ambitions to develop a globally competitive semiconductor sector.

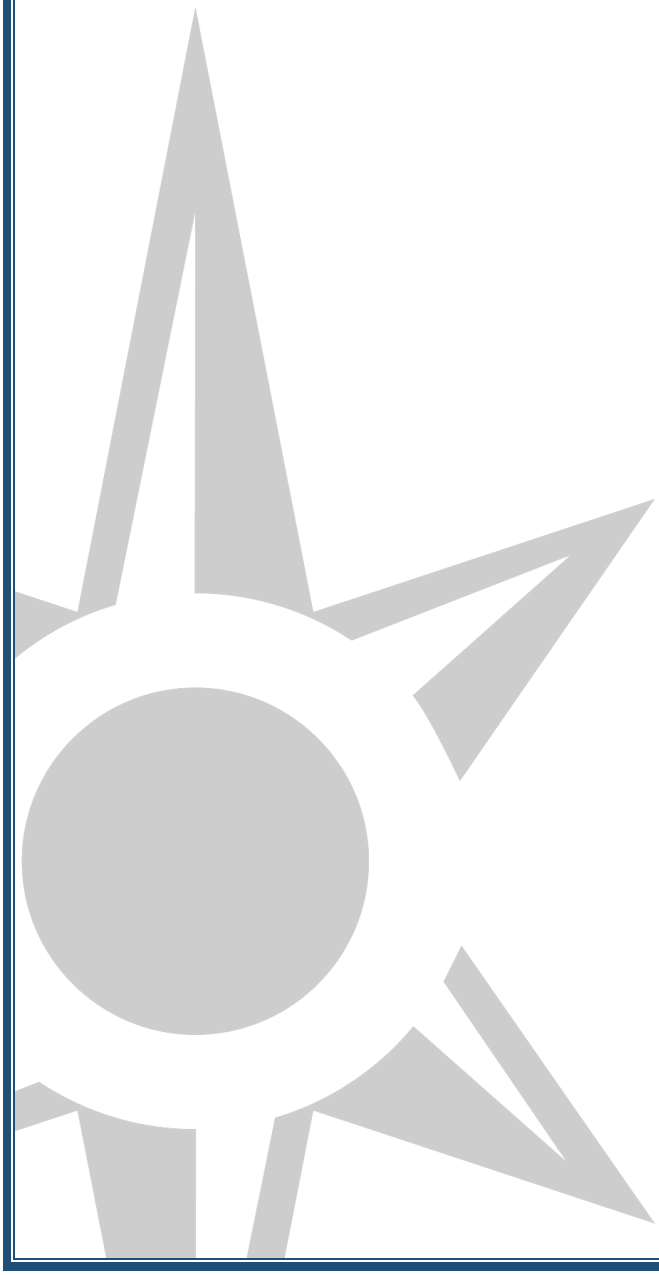
ABOUT THE AUTHOR

HUONG TRAN is the Managing Partner of AIIP, an Intellectual Property Agency in Vietnam, with over 20 years of experience in intellectual property law and practice. Her career spans both the public and private sectors, providing her with extensive insight into Vietnam's IP system, legal framework, and enforcement mechanisms. She holds a Master's degree in Public Policy from Fulbright University Vietnam. Her research and professional interests center on emerging legal frameworks related to science, technology, and intellectual property, as well as the role of innovation in strengthening Vietnam's regional and international competitiveness. Ms. Tran is an Accredited Mediator with the UK-based Center for Effective Dispute Resolution (CEDR). She is also a member of the Vietnam Bar Federation (VBF) and serves as Deputy Head of the Foreign Affairs Department at the Vietnam International Commercial Mediation Center (VICMC).

PACIFIC FORUM
INTERNATIONAL

Vietnam's Strategic Trade Controls in the Semiconductor Sector: Enhancing Trade Coherence and Balancing Compliance Friction for Foreign Investment

By
Doan Quoc Dung



Executive Summary

Doan Quoc Dung

Vietnam is positioning itself as a trusted node in the global semiconductor supply chain, supported by growing foreign direct investment (FDI), an extensive network of free trade agreements (FTAs), and an ambitious national semiconductor strategy. Decree No. 259/2025/ND-CP on Strategic Trade Controls (STCs) strengthens this effort by establishing controls over dual-use goods, end-users, licensing, and corporate Internal Compliance Programs (ICPs). This report finds that these controls are not simply barriers to trade: credible STCs are increasingly a prerequisite for attracting advanced semiconductor technology and investment by assuring foreign partners that sensitive equipment, software, and intellectual property will not be diverted to unauthorized end-users. However, the current framework also generates significant compliance friction. Vietnam's reliance on broad Harmonized System (HS) classifications, decentralized licensing across multiple ministries, and extensive end-user verification requirements contribute to costly delays. Survey findings indicate that individual licenses can take 24–30 days to process, while classification disputes can add another 9–18 days. These burdens disproportionately affect domestic SMEs and new market entrants and can undermine the just-in-time supply chains on which semiconductor production depends.

Vietnam therefore faces a policy challenge of maximizing the economic and security benefits of STCs while minimizing unnecessary regulatory friction. FTA preferences under agreements such as the EVFTA, CPTPP, and RCEP provide substantial advantages to semiconductor exporters, but their value can be diminished when firms face unpredictable licensing and compliance delays. To improve this balance, Vietnam should establish accelerated or provisional licensing for firms with demonstrated compliance maturity; better align its control lists with technically precise international classification standards, including Export Control Classification Numbers (ECCNs); strengthen inter-agency coordination through the Vietnam National Single Window; and provide targeted compliance assistance to domestic SMEs. Properly implemented, Decree 259 can function as a trade enabler rather than a conventional non-tariff barrier—strengthening safeguards against illicit technology diversion while increasing the regulatory trust necessary to attract high-value FDI and advance Vietnam's long-term semiconductor ambitions.

The Changing Global Economy and High-Tech Governance

Global trade is shifting rapidly as countries leverage their supply chains for political gain and deliberately separate core technology ecosystems. Within this volatile environment, the Socialist Republic of Viet Nam is transitioning its economic model by moving away from basic manufacturing and focusing on advanced, high-value technological integration. A central part of this shift is the government's highly structured plan to secure a permanent node in the global semiconductor market. Vietnam supports this goal through deep ties to global trade, backed by 17 active free trade agreements (FTAs) and a verified history of drawing in foreign direct investment (FDI)[1]. Current empirical data shows the country has successfully brought in approximately $11.6 billion in registered capital across 174 discrete semiconductor projects, securing anchor commitments from industry leaders like Intel, Amkor, and Hana Micron[2].

The semiconductor sector occupies the forefront of modern technology. It provides the foundational hardware for consumer electronics, advanced artificial intelligence (AI), and next-generation military applications. Consequently, the industry relies entirely on moving highly sensitive dual-use items across borders quickly and securely. These operational inputs include advanced extreme ultraviolet (EUV) lithography equipment, precision metrology sensors, specialty chemical precursors, and proprietary integrated circuit (IC) designs. Multinational corporations (MNCs), particularly those domiciled in the United States and the European Union, operate under strict extraterritorial export controls, including the US' Export Administration Regulations (EAR) and the EU Dual-Use Regulation. For these corporations to transfer advanced intellectual property and capital equipment to their Vietnamese subsidiaries or foundry partners, Vietnam is required to maintain a comprehensive regulatory environment. The host government must guarantee that sensitive technologies will not be diverted to unauthorized military end-users or sanctioned entities[3].

Recognizing this baseline geopolitical requirement, the Vietnamese government enacted Decree No. 259/2025/ND-CP on Strategic Trade Controls (STCs)[4], which took effect on Oct. 10, 2025[5]. This legal framework introduces mandatory licensing protocols for dual-use items and officially recognizes the institutional role of internal compliance programs (ICPs) for commercial entities trading controlled goods. The implementation of this new decree establishes the necessary legal foundation for technology governance yet simultaneously introduces an additional layer of mandatory regulatory requirements for companies operating in this sector. The administrative obligations associated with these new rules create measurable compliance friction.

Policymakers face the continuous task of balancing the economic integration driven by FTAs with the national security mandates imposed by STCs. Decree 259 operates as a trade enabler rather than a conventional non-tariff barrier. While STCs introduce compliance burdens, the absence of a reliable framework effectively locks a jurisdiction out of global high-tech supply chains. Documented STC compliance is the requisite condition for attracting top-tier FDI and realizing FTA tariff benefits in highly sensitive sectors.

This research report provides an empirical analysis of the net-benefit calculus currently facing Vietnam. The study evaluates the structural mechanisms of Decree No. 259/2025/ND-CP, benchmarks its compliance protocols against global standards, and measures the resulting administrative burdens with established economic models. Furthermore, the report examines the legal boundaries of national security exceptions within major trade agreements. The central policy challenge is determining the optimal equilibrium between fulfilling international non-proliferation obligations and minimizing operational friction to

[1] Resolution No. 59/NQ-CP (2025) on International Integration in the New Context

[2] Dunning, J. H. (2000). The eclectic paradigm as an envelope for economic and business theories of MNE activity. International Business Review; Narula & Dunning (2010). Multinational enterprises, development and globalization: Some clarifications and a research agenda

[3] Law on Technology Transfer (Law No. 80/2006/QH11, as amended 2017) and the Law on Intellectual Property (Law No. 50/2005/QH11, as amended 2022); Atlas. (2025). Intellectual Property Law in the Semiconductor Industry: Key Considerations for Businesses

[4] Baker McKenzie. (2025). Vietnam: Draft decree on strategic trade control. InsightPlus.

[5] Government of Vietnam, Decree No. 259/2025/ND-CP on Strategic Trade Controls

sustain the country's comparative advantage for future FDI.

Deciphering Vietnam's National Semiconductor Blueprint

An analysis of Vietnam's trade controls requires contextualizing them within the state's broader industrial policy. This framework was formally codified on Sept. 21, 2024, when the prime minister signed Decision No. 1018/QD-TTg, launching the "National Strategy for the Development of Vietnam's Semiconductor Industry to 2030, with a vision to 2050"[6]. The strategy operates on a core conceptual architecture defined by the macroeconomic formula C = S + E + T + 1. Within this framework, C represents the overarching chip industry. S stands for Specialized Application-Specific Integrated Circuits (ASICs). E is the foundational electronics manufacturing base necessary to support domestic semiconductor consumption. T represents a national mandate for talent development. Finally, the +1 positions Vietnam as a secure, politically reliable, and technologically compliant alternative destination in the global supply chain, designed specifically to capture capital flight resulting from the ongoing US-China technological bifurcation.

The roadmap detailed in Decision 1018/QD-TTg is sequenced into three distinct operational phases. Each phase features specific developmental milestones designed to elevate Vietnam from a downstream assembly node to an upstream innovation hub.

Table 1: Three Developmental Phases of Vietnam's National Semiconductor Roadmap

Phase	Timeline	Objective	Targets
Phase 1: Foundational Integration	2024 to 2030	Leverage geopolitical advantages to selectively attract high-value FDI. Establish at least 100 domestic semiconductor design enterprises, 1 small-scale foundational manufacturing plant, and 10 advanced packaging and testing facilities.	Achieve an annual semiconductor industry revenue exceeding $25 billion with an added value growth rate of 10-15% while cultivating a specialized workforce of over 50,000 engineers.
Phase 2: Global Centrality	2030 to 2040	Transition the domestic ecosystem into a globally recognized semiconductor and electronics hub.	Develop deep domestic industrial capabilities that seamlessly blend sovereign self-reliance with highly compliant FDI networks. Move beyond basic packaging into advanced logic and memory fabrication.
Phase 3: Innovation Leadership	2040 to 2050	Achieve status as a premier global leader in semiconductor and electronics manufacturing.	Master core research and development across advanced microelectronics fields, driving proprietary technological breakthroughs.

Executing this phased strategy requires substantial infrastructure scaling and resource mobilization. The state designated the National Innovation Center alongside three premier high-tech zones situated in Hanoi, Ho Chi Minh City, and Da Nang as the physical anchors for the ecosystem. These localized hubs are structured to host pilot fabrication facilities, advanced packaging laboratories, and chip design training centers. The intent is to bridge the gap between academic theory and industrial application. Among these hubs, Da Nang sets itself apart as Vietnam's primary regulatory sandbox for

[6] Government of Vietnam, Decision No. 1018/QD-TTg (2024) on National Strategy for the Development of Vietnam's Semiconductor Industry to 2030, with a vision to 2050

semiconductors. Through leveraging specific legislative mechanisms, primarily Resolution No. 259/2025/QH15, Da Nang bypasses standard provincial limits to pilot urban governance policies[7]. This created a specialized legal framework designed to accelerate high-tech investment by bypassing standard provincial regulatory limitations, including direct land allocation for chip facilities without competitive auctions, 150% tax deductions on semiconductor R&D, 5-year income tax exemptions for chip design experts, and up to 5% direct subsidies for capital equipment and production relocation.

Concurrently, Vietnam is attempting to leverage its natural resource endowments to build upstream supply chain resilience. Geological surveys indicate the country possesses an estimated 22 million metric tons of rare-earth reserves, positioning it among the top global sources of these critical minerals. While historical annual production was constrained to approximately 300 tons, national resource strategies implemented in 2025 aim to scale output to between 20,000 and 60,000 tons annually by 2030. Because rare earth elements are necessary for advanced semiconductor manufacturing, this mineral wealth provides Vietnam with strategic geoeconomic leverage. The extraction, processing, and subsequent exportation of high-purity rare earth materials directly trigger the jurisdictional oversight of global non-proliferation regimes and domestic trade controls. These materials possess inherent dual-use capabilities applicable to military technologies. The physical expansion of the semiconductor industry dictates that regulatory oversight must expand proportionally.

The Legislative Architecture of Decree No. 259/2025/ND-CP

To align its domestic legal environment with the expectations of technology partners and to fulfill non-proliferation obligations under United Nations Security Council mandates, the Vietnamese government overhauled its export control regime. The promulgation of Decree No. 259/2025/ND-CP consolidated prior, fragmented administrative controls into a universally applicable legal basis for managing sensitive technologies.
The operational core of Decree 259 resides in Article 3, which provides legally binding definitions for regulated commerce. Strategic trade goods encompass weapons of mass destruction (WMD), conventional weapons, and dual-use goods used in the development, production, or deployment of such weapons. The legislation specifies that dual-use goods refer to commodities, software, and technologies normally intended for civilian, commercial, or industrial purposes that possess technical characteristics rendering them viable for application in WMD or conventional military programs.

In the context of the semiconductor sector, this dual-use definition is broad. Modern integrated circuit fabrication requires a vast array of operational inputs that fall under this classification. This includes deep ultraviolet (DUV) lithography machines, high-precision chemical vapor deposition (CVD) equipment, encrypted Electronic Design Automation (EDA) software, specialized isotopic precursor gases, and radiation-hardened IC designs capable of withstanding the environments of aerospace applications. Consequently, nearly every phase of the semiconductor manufacturing process interacts with the regulatory perimeters established by the decree.

Rather than centralizing export control authority within a single bureaucratic entity, Decree 259 uses a decentralized, multi-agency licensing framework. This architecture distributes jurisdictional oversight across various specialized ministries based on the technical nature and potential end-use of the controlled item. Annex I of the decree contains granular lists of dual-use goods subject to mandatory licensing.

The jurisdictional distribution is structured as follows:

- **Ministry of Science and Technology (MOST):** This ministry holds primary authority over the most critical components of the semiconductor supply chain. MOST is responsible for announcing detailed lists of dual-use technologies and issuing licenses for radioactive materials, nuclear equipment, high-performance electronics, advanced computing systems, telecommunications infrastructure, and precision sensors. For semiconductor fabrication plants operating in

[7] Resolution No. 57/NQ-CP (2025) on continuing institutional and policy improvements to promote science, technology, innovation, and digital transformation

Vietnam, MOST is the primary regulatory gatekeeper for the importation and subsequent re-exportation of advanced fabrication machinery and metrology equipment.

- **Ministry of Industry and Trade (MOIT):** MOIT functions as the overarching coordinator for strategic trade while maintaining specific licensing authority over dual-use specialty metals and the complex precursor chemicals heavily utilized in semiconductor etching and deposition processes.
- **Ministry of Construction (MoC) and Ministry of Health (MoH):** While less directly involved in daily semiconductor operations, these ministries manage dual-use items related to aerospace, maritime applications, and biochemical products.

For MNCs, this decentralized structure requires the implementation of sophisticated internal trade compliance routing. A comprehensive semiconductor manufacturing facility may simultaneously require active licenses from MOIT for ultra-pure hydrofluoric acid used in etching and entirely separate licenses from MOST for the optical sensors utilized in quality control. This multi-agency requirement increases administrative complexity during the procurement phase.

Structural Misalignment: HS Codes vs. ECCN in Global Trade

A primary source of compliance friction within Decree No. 259/2025/ND-CP stems from a structural misalignment between Vietnam's domestic classification methodology and the internationally recognized standards for dual-use goods.

Globally, advanced strategic trade control regimes, particularly those of Wassenaar Arrangement-participating states, rely on the Export Control Classification Number (ECCN) system. The ECCN system classifies items based on precise technical parameters, software capabilities, and technological performance thresholds. Conversely, Annex I of Vietnam's Decree 259 relies heavily on the Harmonized System (HS) nomenclature, which was fundamentally designed by the World Customs Organization for determining import tariffs based on an item's physical material composition rather than its technical capability.

Applying HS codes to dual-use semiconductor technology creates systemic over-capture. The HS system lacks the granularity required to differentiate between a benign commercial product and a highly restricted military-grade technology if both are constructed from similar materials or serve a similar general function.

For example, both a standard, decades-old wafer cleaning machine used in legacy manufacturing as well as a state-of-the-art EUV lithography machine critical for advanced AI chip fabrication may fall under identical or highly similar HS codes related to semiconductor manufacturing equipment. Under the ECCN system, the legacy machine is subject to minimal controls, while the EUV machine is subject to severe national security restrictions.

Because Decree 259 triggers licensing requirements based on these broad HS categories, customs authorities and licensing ministries process a high volume of applications for benign items. Firms are legally required to halt shipments of standard commercial equipment to undergo a manual technical review by MOST or MOIT simply because the general HS code matches a category in Annex I. This structural misalignment forces MNCs into an expensive cross-functional response: compliance teams must routinely pull highly compensated R&D and engineering staff away from core innovation to draft technical defense documents and explain specialized specifications to government reviewers. This misallocation of high-cost talent across multiple departments, redirecting key R&D personnel from product development to regulatory defense, drives the administrative delays and elevated operational costs identified in current empirical surveys.

Catch-All Provisions: The Shift Toward End-Use and End-User Controls

While the classification of goods represents the first pillar of STCs, the global regulatory landscape has shifted focus toward the specific use and user of the technology. Decree No. 259/2025/ND-CP formally integrates these concepts into Vietnamese law through comprehensive catch-all provisions.

Strategic trade controls account for the fact that analyzing the physical product is insufficient. A civilian-grade semiconductor component that is completely uncontrolled on Annex I can become a strategic threat if it is knowingly sold to a foreign

military intelligence agency for use in a guidance system. Consequently, Article 6 of Decree 259 places an affirmative legal duty on traders to halt transactions. They must immediately notify MOIT and the Ministry of National Defence if they detect or reasonably suspect that uncontrolled goods are intended for production of WMDs or military applications.

This shifts the regulatory burden from list-based compliance to behavioral and transactional compliance. Firms operating in Vietnam must implement rigorous end-user screening (EUS) protocols. This requires systematic vetting of all consignees, purchasing agents, logistics providers, and final end-users against global denied-party lists prior to order fulfillment.

The primary compliance challenge for semiconductor firms in Vietnam is the proliferation of procurement proxies or front companies. A domestic enterprise may attempt to purchase advanced ICs or semiconductor manufacturing equipment, and the firm itself may not appear on any US, EU, or UN sanctions list. However, if the firm acts as a procurement proxy intending to transship the technology to a restricted entity in a neighboring jurisdiction, the MNC supplying the equipment assumes severe legal liability under extraterritorial laws.

To manage this risk, Decree 259 mandates the use of detailed end-user certificates (EUCs). An EUC is a legally binding document signed by the final buyer certifying the intended civilian use of the item and guaranteeing it will not be re-exported without prior state authorization. For MNCs, verifying the authenticity of these EUCs and investigating the corporate structures of domestic buyers requires investment in automated screening software and specialized compliance personnel, adding another layer of quantifiable friction to operational supply chains.

Operationalizing Controls: Licensing Modalities and Customs Integration

Decree 259 mandates that any trader engaging in the export, temporary import for re-export, border-gate transfer, transshipment, or transit of dual-use goods listed in Annex I must secure formal licenses from the relevant ministry prior to initiating the physical movement of the goods. The legislation constructs a two-track licensing system deliberately designed to balance the state's need for strict, granular oversight with the economic necessity of providing operational facilitation for highly compliant, low-risk actors.

1. **Individual Shipment License (The Default Modality):** This foundational license type is valid for a maximum of three months from the date of official issuance and applies exclusively to a single shipment of dual-use goods. This modality is designed for ad-hoc transactions, highly sensitive technological transfers, or entities that have not yet demonstrated advanced compliance maturity. For semiconductor firms reliant on just-in-time (JIT) manufacturing and dynamic supply chains, being constrained to per-shipment licensing represents a severe operational bottleneck. Any delay in license approval can halt a multimillion-dollar production line.
2. **Term-Based (12-Month) License (The Facilitation Modality):** Recognizing the need for trade facilitation, the decree introduces a term-based license. This highly coveted authorization is valid for 12 months and permits an unlimited number of exports, temporary imports for re-export, transits, or transshipments of specified goods during its validity period. Access to this perk, however, is heavily restricted. Application for a term-based license is strictly contingent upon the trader holding a formal decision from the state certifying the successful implementation of an Internal Compliance Program (ICP) for a minimum of two years.

To mitigate the inherent administrative delays of paper-based licensing, Article 6 of the Decree mandates a rapid digital transformation. The legislation dictates that within six months of the decree's effective date (essentially, by April 2026) all designated licensing agencies must fully coordinate with the Ministry of Finance to execute all licensing procedures electronically through the Vietnam National Single Window (VNSW) portal[8].

Under this modernized regime, traders are required to complete detailed declaration processes for every shipment of dual-use goods directly on the VNSW

[8] Law No. 90/2025/QH15 amending the Customs Law, the VAT Law; Vietnam Investment Review (VIR) (2025) Customs reform to prioritise high-tech and innovative businesses.

portal prior to initiating standard physical customs procedures at the border or port. The assigned ministries review these digital declarations and grant electronic approvals, which subsequently serve as legally binding documentation for the general customs clearance process. The decree carves out an operational exception to incentivize corporate compliance through the term-based license model. Through this model, traders who have been formally approved as meeting the requirements of a certified ICP may be exempted from certain granular, per-shipment declaration requirements, accelerating their supply chain velocity.

Internal Compliance Programs as the Vanguard of Trade Security

Formally including the ICP into Decree 259 represents Vietnam's definitive alignment with international non-proliferation best practices. By legally recognizing ICPs, the state effectively offloads the immense administrative burden of day-to-day risk management from state agencies directly onto the corporate actors facilitating the trade. An ICP is legally defined by the Decree 259 as a formalized, rigorously documented set of internal corporate procedures established by traders to ensure absolute adherence to trade control regulations across all phases of handling dual-use goods.

To access the trade facilitation benefits of the 12-month term license and customs declaration exemptions, traders must undergo a rigorous state-sponsored certification process. A trader claiming to have successfully implemented an ICP must submit a highly detailed dossier to MOIT for formal review. The regulatory timeline is exceptionally compressed. Within seven working days of receiving a valid dossier, MOIT is legally mandated to coordinate with other relevant ministries, such as MOST or the Ministry of National Defence, to execute a detailed, on-site inspection of the trader's physical business establishment and digital record-keeping systems.

The purpose of this physical inspection is to verify the operational reality of the documented procedures, ensuring the ICP is not merely a theoretical paper construct. Upon successful verification of the compliance architecture, MOIT issues a formal decision certifying the ICP implementation. This certification is valid for a period of five years, after which it must be comprehensively renewed. If the inspection reveals systemic weaknesses, MOIT will issue a formal written refusal explicitly stating the reasons for denial, forcing the firm back into the highly restrictive 3-month individual licensing regime.

Decree 259 strictly mandates that the ICP contain verifiable procedures. The precise architectural requirements for these programs are detailed extensively in Appendix II of the legislation. These requirements mandate the creation of strict protocols for information storage, physical and digital document retention, and the fulfillment of mandatory state notification obligations. Article 6 places an affirmative legal duty on traders to immediately notify MOIT and the Ministry of National Defence if they detect or even reasonably suspect that goods they are trading are being diverted for the production of WMDs, or if the recipients are identified on designated restricted party lists.

The operational expectations embedded in Vietnam's ICP framework closely mirror the core elements of established global Strategic Trade Schemes (STS)[9], ensuring interoperability with the compliance departments of Western MNCs. According to established STS best practices, a viable ICP must address several critical vectors of corporate governance:

Table 2: Vietnam's Internal Compliance Programs framework

Core ICP Element	Implementation Requirement for Semiconductor Firms	Global Equivalency Alignment
End-User and Consignee Screening	Mandatory, systematic vetting of all consignees, purchasing agents, and final end-users against global denied-party lists prior to order fulfillment or technology transfer.	Directly aligns with US EAR Entity List screening requirements and the catch-all controls stipulated in EU Regulation 2021/821.

[9] Primakov, D. (2023). Perspective Chapter: Models of Sanctions Compliance and Regulatory Expectations. Corruption - New Insights.

Comprehensive Record Keeping	Maintenance of immutable audit trails, internal technical classification assessments, subsidiary instructions, and explicit directives issued to third-party freight forwarders.	Meets the stringent administrative retention standards mandated by the Wassenaar Arrangement for dual-use technologies.
Continuous Awareness and Training	Systematic, documented education of procurement, logistics, and sales personnel regarding evolving dual-use technology thresholds and red-flag identification.	Serves as a standard requirement under European corporate governance models (such as Commission Recommendation (EU) 2019/1318 or Germany's BAFA ICP Guidelines) for preventing inadvertent technology diversion.
Independent Internal Audits	Execution of regular, independent internal reviews utilizing standardized checklists to verify that operational procedures are effectively isolating and halting non-compliant transactions.	Fully complies with the rigorous audit mandates necessary for securing European Union Global Export Authorizations (EUGEA).

This structural alignment is of paramount geopolitical importance right now. The global regulatory landscape is aggressively tightening around foundational semiconductor technologies. On Sept. 8, 2025, the European Commission adopted a Delegated Regulation comprehensively updating Annex I of the EU dual-use export control list, expanding controls into emerging fields deemed high-risk for European security. This added new entries for quantum computing systems, cryogenic components, and tightened restrictions on advanced semiconductor manufacturing equipment. Regional actors are escalating their oversight as well. Additionally, India recently issued a sweeping revision of its SCOMET list, introducing an entirely new Category 7 specifically targeted at emerging technologies, including cryogenic CMOS circuits and next-generation lithography machines capable of sub-45 nm fabrication. China has also bolstered its export control regulations over dual-use items. By institutionalizing a world-class ICP framework, Vietnam effectively assures Western partners that highly sensitive technological inputs exported to Vietnamese fabs will not be illegally diverted to unauthorized end-users. This safeguards Vietnam's position as a trusted and legally insulated node in the global supply chain.

The Net-Benefit Calculus: Benchmarking FTA Gains Against Trade Control Friction

To understand the economic impact of Decree 259, policymakers measure the net-benefit calculus. This involves evaluating whether the direct financial and market access gains of FTAs outweigh the new compliance burdens. For Vietnam's semiconductor industry [10], this is benchmarked using macroeconomic use metrics mapped against the dual-use regulatory friction.

Based on trade data for the 2025-2026 cycle, the direct financial benefit of FTAs for a semiconductor firm in Vietnam remains substantial. The primary metric is the Net Tariff Advantage (NTA).

Equation 1: Net Tariff Advantage (NTA) [11]

NTA = Export Value x (Average MFN Tariff Rate - FTA Preferential Rate)

Gross export value for ICs (HS 8542) alone accounted for an estimated $31.5 billion. The average global most-favored-jation (MFN) tariff sits between 8.3% and 9.5%. Under new-generation agreements like the

[10] Baldwin, R. (2016). The great convergence: Information technology and the new globalization. The Belknap Press of Harvard University Press

[11] Nicita, A. (2013) Measuring the relative strength of preferential market access. Policy Issues in International Trade and Commodities Study Series No. 48. Geneva: United Nations Conference on Trade and Development; Cipollina, M., Salvatici, L. and Giovannetti, G. (2020) 'The trade effect of the EU's preference margins and non-tariff barriers', Journal of Risk and Financial Management.

EU-Vietnam Free Trade Agreement (EVFTA), the Comprehensive and Progressive Agreement for Trans-Pacific Partnership (CPTPP), and the Regional Comprehensive Economic Partnership (RCEP), the preferential rate drops to exactly 0%. Applying the NTA equation identifies a window of $2.6 billion to $3 billion in annual industry-wide tariff savings. For an individual firm, the benchmark net benefit before factoring in STC compliance costs equates to roughly $830,000 to $950,000 in tariff savings for every $10 million of exported semiconductors.

These benefits vary wildly depending on the specific regional partner and the corresponding trade agreement. The breakdown below illustrates this mathematical calculus across three key global markets.

Table 3: Net-Benefit of FTA Gains across 3 Integrated Circuits Markets of Vietnam

Region / Partner	Applicable Trade Agreement	Average MFN Tariff	Applied Preferential Rate	Strategic Trade Impact
European Union	EVFTA	~8.3% to 9.5%	0%	Provides an exceptionally strong financial benefit. Electronics exports surged 66.9% in 2024 to $11.2 billion. Eliminates almost all tariffs, giving companies in Vietnam a massive competitive edge.
Asia (Regional)	RCEP	~8.3% to 9.5%	0%	High volume impact. Supports a $140 billion broader electronics base by removing fees on critical components from Japan and South Korea used for local assembly.
United States	None (Bilateral Terms)	20% (Reciprocal)	20%	The US remains the largest importer ($6.2 billion in 2024) but lacks an FTA. The heavy 20% reciprocal tariff highlights the comparative luxury of the 0% rates locked in by the EVFTA and CPTPP.

While the potential financial benefit is high, the actual capture of these benefits, measured as the Preference Utilization Rate (PUR), is the true benchmark. Currently, Vietnam's overall national FTA utilization rate hovers around 37%. For the semiconductor sector, dominated by FDI entities capable of meeting strict rules of origin, the realistic benchmark target is closer to 45% or 50%. Reaching this target requires firms to execute a dual-track check. Compliance officers must check the primary semiconductor HS Codes against the FTA tariff schedule to secure the 0% rate. They must simultaneously cross-reference that code against Annex I of Decree 259 to determine if an MOIT or MOST export license is required. The simplification benefit of the decree is that traders who complete the 2-year ICP maturation period receive expedited term licenses, reducing per-shipment friction and supporting higher PUR targets.

Quantifying Regulatory Friction Through the Standard Cost Model

Accessing FTA benefits requires navigating the mandatory regulatory requirements imposed by Decree 259. To rigorously quantify this friction, advanced analytical frameworks such as the Standard Cost Model (SCM) are utilized. The SCM provides an internationally recognized methodology for measuring the administrative burdens and compliance costs imposed by state legislation[12].

[12] Wang, C. (2019). Invocation of National Security Exceptions under GATT Article XXI: Jurisdiction to Review and Standard of Review. Chinese Journal of International Law.; Danciu, D.-M., Martens, L., & Marneffe, W. (2024). Assessing the quality of European Impact Assessments. European Journal of Risk Regulation.; Petrenko, Y., Denisov, I., Koshebayeva, G., & Biryukov, V. (2020). Energy

The SCM methodology calculates the Total Administrative Burden by deconstructing broad administrative activities into cost variables. The core calculation integrates the internal time required to complete tasks, the hourly wage of the internal personnel, external fees for consultants, and the annual frequency of the required transactions.

Equation 2: Standard Cost Model (SCM) for STC Compliance [13]

Total Administrative Burden = Sum of [(Internal Time x Hourly Wage) + External Costs] x Annual Frequency

When the bottom-up approach of the SCM equation is applied to the semiconductor sector operating under the parameters of Decree 259, several major new cost vectors become apparent. The breakdown below illustrates how different aspects of administrative burden align with the variables in the SCM calculus.

Table 4: Variables in the Standard Cost Model for STC Compliance

Aspect of Administrative Burden	SCM Cost Drivers	Operational Impact and Friction
Product Classification	Internal Time, Hourly Wage	High continuous cost. Requires highly compensated systems engineers to painstakingly cross-reference massive bills of materials against specific HS codes and technical performance thresholds.
ICP Architecture Requirements	Capital Expenditure, Internal Time	Involves hidden annoyance costs. Requires automated software for real-time end-user screening. Includes the institutional drag of halting physical shipments to manually investigate false positives.
State Audits and Inspections	External Costs, Operational Pauses (excluded from baseline SCM calculations)	Introduces massive external transaction costs. Firms frequently retain external legal counsel to navigate the 7-day multi-agency inspection process, risking manufacturing floor pauses. These ad-hoc external fees and potential downtime costs represent qualitative operational risks and are excluded from baseline SCM calculations due to their high variability

The policy challenge identified through the SCM is the friction-facilitation paradox. The semiconductor sector relies on extreme temporal precision. A bureaucratic delay in securing an individual 3-month shipment license for a critical precursor chemical possesses the potential to halt a fabrication line, resulting in financial losses.

The structural limitation in the state's facilitation mechanism is the mandatory incubation period. Until a firm officially qualifies for the 12-month term license, which requires two full years of certified ICP operation, it is subjected to the rigid 3-month individual licensing regime. For new FDI entrants, this 2-year maturation period represents an operational hurdle. The time expenditure and documentation complexity erode the efficiency derived from FTA provisions. The risk is that high administrative friction may alter the investment calculus of MNCs.

Beyond the Balance Sheet: The Non-Monetary Benefits of Trade Controls

When evaluating the friction of the SCM metrics against FTA tariff savings, analysis must extend beyond immediate financial compliance costs. A strong STC framework generates non-monetary benefits across the economic ecosystem that provide justification for the administrative burden. For the government, implementing STCs elevates the country's standing within international diplomatic and security architecture. It demonstrates that the state is a responsible actor capable of safeguarding dual-use goods, leading to deeper strategic partnerships. The framework also acts as a national shield. It reduces the risk that domestic companies

Efficiency of Kazakhstan Enterprises: Unexpected Findings. Energies.

[13] International SCM Working Group (IWGAD) 2004, The Standard Cost Model: A framework for defining and quantifying administrative burdens for businesses.

will inadvertently violate international sanctions, which could trigger secondary sanctions against Vietnam's broader economy. It also provides the state with mechanisms to monitor where critical technologies are flowing, aiding in the prevention of unauthorized technology transfer.

Global firms gain essential supply chain predictability and legal certainty in jurisdictions with enforced Strategic Trade Controls (STCs). Strict STCs safeguard advanced manufacturing equipment and intellectual property against unauthorized diversion to unverified end-users. Furthermore, when Vietnam's framework aligns with home-country export controls, it eliminates regulatory friction and secures seamless intra-company transfers.

Small and medium-sized enterprises (SMEs) experience a degree of forced modernization and governance spillover that delivers direct, commercial advantages in high-tech markets[14]. To comply with STCs and secure ICP certification, local SMEs must upgrade their IT systems, record-keeping protocols, and corporate governance structures. While this transformation requires upfront investment, it yields immediate returns by drastically lowering transaction costs and eliminating liability barriers for foreign buyers. A local SME that achieves STC compliance transitions from a generic vendor into a verified tier-1 partner. Crucially, certified compliance enables SMEs to qualify for streamlined 12-month multi-shipment licenses, avoiding the delays of shipment-by-shipment approvals while giving MNCs the legal protection required to integrate them into specialized supply chains for high-value components. Far from an administrative deadweight, documented compliance with international trade controls functions as a commercial accelerator and an essential prerequisite for SMEs expanding into heavily regulated Western markets.

For the broader supply chain ecosystem, consistent enforcement creates systemic de-risking. Broad STC enforcement ensures that negligent actors cannot easily contaminate the regional network, protecting the ecosystem's collective reputation.

Empirical Findings: Compliance Cost Validation

To systematically operationalize the SCM and scientifically capture the quantitative compliance costs introduced by Decree 259/2025/ND-CP, a targeted fieldwork methodology was deployed. The data gathered from commercial entities, regulatory bodies, and logistics providers reveals systemic friction and notable asymmetric burdens across the sector.

The data demonstrates that the compliance architecture disproportionately impacts domestic SMEs and localized Outsourced Semiconductor Assembly and Test (OSAT) facilities compared to Tier-1 MNCs. Tier-1 manufacturers possess the internal scale to absorb the administrative burden. According to the survey data, Tier-1 MNCs dedicate an average of 115 to 160 hours per month purely to product classification. They compensate specialized trade compliance officers at a premium rate averaging $31.00 to $38.50 per hour. Consequently, Tier-1 firms rely less on external consultants, outsourcing only 15% to 30% of their compliance activities, resulting in average annual external legal costs ranging between $90,000 and $145,000. Their capital expenditure for deploying automated ICP software architectures averages $260,000 to $420,000.

Conversely, domestic chip design startups and local OSATs lack internal technical capacity. Domestic firms average only 30 to 65 classification hours internally because they are forced to outsource an average of 60% to 90% of their compliance operations to external trade consultants and law firms. Despite this heavy outsourcing, domestic firms face external costs averaging $55,000 to $140,000 annually, alongside capital expenditures averaging $70,000 to $210,000. For an emerging domestic startup, diverting nearly $150,000 in Year 1 purely to regulatory compliance rather than research and development represents an operational barrier to entry. This validates the hypothesis that Decree 259 risks causing market consolidation.

The empirical data also validates that the structural misalignment between Vietnam's HS-based control list and the global ECCN standard generates operational friction. On a scale of 1 to 5, Tier-1 MNCs rated the friction caused by HS misalignment at an average of 4.4. This friction is compounded by the new end-user screening requirements. Tier-1 MNCs expend an average of 85 to 120 additional hours per month solely verifying end-user certificates and tracing corporate ownership structures to ensure

[14] Resolution No. 68/NQ-CP (2025) on promoting private economic sector development

compliance with behavioral mandates. Logistics providers reported that securing and verifying authentic EUCs introduces an average delay of 3 to 9 days into the shipping cycle.

Data collected from regulatory authorities confirms that the decentralized, multi-agency framework contributes to the friction-facilitation paradox. Processing times for a standard 3-month individual shipment license currently average 24 to 30 days across MOIT, MOST, and Customs divisions. When a highly complex dual-use item triggers a classification dispute, resolving the HS code discrepancy requires an average of 9 to 18 additional days of inter-agency consultations. End-user advisory verifications by the Ministry of National Defence or the Ministry of Public Security require an average of 18 to 21 days. For a semiconductor firm relying on JIT manufacturing, a combined processing and verification delay fundamentally negates the supply chain velocity benefits negotiated in the CPTPP or EVFTA. Indeed, MNCs rated the impact of the current STC regime on their JIT schedules at an average severity of 3.9 out of 5.

Reconciling Strategic Controls with Free Trade Agreement Coherence

Vietnam's network of seventeen FTAs serves as the macroeconomic mechanism for integrating its semiconductor sector into global markets. The imposition of trade-restrictive measures through Decree 259 requires a legal examination of how these domestic security controls interact with international economic integration instruments. The implementation of STCs must be analyzed against the foundational FTA principles of market transparency, non-discrimination, and the invocation of national security exceptions.

Bilateral and multilateral trade agreements are designed to promote open markets, eliminate tariffs, and reduce non-tariff barriers. However, these agreements can also contain specific provisions that allow sovereign states to prioritize national security obligations over the mandates of pure trade liberalization.

The CPTPP features a broad security exception under Article 29.2. This provision states that nothing in the agreement shall be construed to require a member party to furnish information if the state determines that such disclosure would be contrary to its security interests. It does not preclude a party from applying measures that it considers necessary for the fulfillment of obligations with respect to the maintenance of international peace or security. This provision is intentionally broad and provides the Vietnamese state with sovereign policy space to enforce the licensing of dual-use semiconductor technologies without violating CPTPP market access commitments.

The RCEP incorporates security exceptions under Article 17.13 that mirror the language of the CPTPP. The RCEP text ensures that governments are empowered to take actions deemed necessary to protect national security interests. RCEP Article 10.15 repeats these security exceptions within the context of the investment chapter. This repetition ensures that FDI protections and investor-state dispute settlement mechanisms cannot override state-mandated strategic controls.

The EVFTA operates under the protective umbrella of security exceptions derived from the foundational texts of GATT Article XXI and GATS Article XIV bis. The European Union routinely updates its domestic dual-use export control lists under Regulation 2021/821 to include quantum computing and advanced semiconductor manufacturing equipment. This reinforces the normative global acceptance of utilizing security-based logic to justify trade restrictions. Within the EVFTA, a panel of experts handles complex disputes, providing a structured mechanism for resolving normative trade conflicts should the EU challenge Vietnam's implementation of controls.

While Article 29.2 of the CPTPP and Article 17.13 of RCEP provide a legal foundation for the enactment of Decree 259, leveraging these exceptions carries systemic risk. International trade jurisprudence, influenced by World Trade Organization panel reports such as the Russia-Traffic in Transit case, indicates that national security exceptions are subject to review [15]. Measures must bear a plausible relationship to actual security threats rather than functioning as veiled protectionism. Legal analysis notes that the concept of essential security has evolved to encompass complex cyberthreats and the protection of sovereign infrastructure.

[15] Wang, C. (2019). Invocation of National Security Exceptions under GATT Article XXI: Jurisdiction to Review and Standard of Review. Chinese Journal of International Law.

For the Vietnamese government, the primary risk of non-compliance with its FTA network lies in the precise mechanics of STC application. If the decentralized, multi-agency licensing process involving MOIT and MOST becomes deeply opaque, delayed by bureaucratic inefficiency, or is perceived to discriminate against specific foreign entities under the guise of national security, it could trigger formal trade disputes.

Regulatory coherence is requisite for Vietnam's strategy. The state must ensure that STC measures are tailored to legitimate threats, transparently administered via the digitized VNSW portal, and limited to genuine dual-use non-proliferation objectives. Utilizing strategic trade controls for domestic industrial protectionism would undermine the regulatory trust required to maintain Vietnam's position within global supply chains.

Second and Third-Order Geopolitical and Supply Chain Implications

The implementation of Decree 259 reshapes the operational environment, initiating second and third-order effects that alter the strategic calculus for MNCs operating within Southeast Asia.

A primary geopolitical effect of the legislation is the enhancement of Vietnam's institutional reputation in key Western capitals. By instituting an STC regime that mandates rigorous ICPs and enforces strict end-user verification protocols, the Vietnamese state mitigates the risk of the jurisdiction serving as a conduit for illicit technology diversion. In the context of the ongoing technological bifurcation between major economic powers, where extraterritorial regulations are utilized to manage advanced semiconductor flows, Vietnam’s regulatory maturation provides Western policymakers with the institutional confidence necessary to authorize the export of advanced technology transfers to Vietnamese fabrication facilities. This regulatory trust supports the objectives of Decision 1018/QD-TTg, establishing Vietnam as a legally insulated destination for capital investment.

A consequential third-order economic effect is the probable consolidation of the domestic semiconductor ecosystem due to the asymmetric compliance burden. The demanding architecture of the ICP requirements, the personnel and financial costs associated with the SCM compliance metrics, and the 2-year waiting period required to transition from 3-month individual licenses to 12-month term licenses establish a formidable barrier to entry for smaller firms. While Tier-1 MNCs possess the resources to absorb administrative burdens, SMEs and emerging domestic chip design startups struggle to navigate the compliance architecture. This dynamic may lead to a concentration of manufacturing and export activity among highly capitalized, incumbent players, potentially stifling grassroots technological innovation.

Operationally, the decree forces logistics providers and customs declaring agents to fundamentally overhaul physical and digital operations. The ICP guidelines mandate that corporations maintain strict records of instructions provided to third-party logistics firms regarding the physical handling, storage, and transport of dual-use goods. This pushes legal liability into the downstream supply chain. Major logistics hubs are forced to implement physically segregated warehousing facilities for Annex I goods to prevent commingling with uncontrolled goods and to ensure access for MOIT or MOST compliance inspectors.

The requirement to clear dual-use goods through the VNSW portal prior to physical customs procedures alters transit times. To compensate for these administrative constraints, procurement managers are forced to expand buffer stocks of critical precursor chemicals, thereby increasing inventory carrying costs and reducing the capital efficiency of operations. On a macro level, alignment with international norms contributes to a broader regional harmonization of non-proliferation controls within ASEAN, encouraging a more secure Southeast Asian trading bloc.

Policy Pathways for Mitigating Compliance Friction

Vietnam’s ambition to ascend the global semiconductor value chain is tied to the state's institutional capacity to balance economic openness with strategic security. Decree No. 259/2025/ND-CP establishes a legal foundation for dual-use technology governance, aligning the nation with global non-proliferation standards. However, the administrative friction introduced by the multi-agency framework poses a quantifiable risk to the operational efficiencies promised by Vietnam's FTA network. To optimize the equilibrium between

sovereign security obligations and foreign investment appeal, specific adaptations are indicated for the regulatory apparatus.

The requirement demanding two years of localized ICP implementation before a firm is eligible to secure a 12-month term license disproportionately affects newly arriving, highly compliant FDI. To alleviate this friction, MOIT should implement an accelerated certification pathway, or issue a provisional term license, tailored for MNCs that already hold validated, top-tier compliance certifications in their home jurisdictions, such as the United States' C-TPAT program, the EU's Authorized Economic Operator (AEO) status, or existing EUGEA compliance. Establishing a framework for the mutual recognition of corporate compliance maturity would reduce regulatory friction for trusted actors.

To address the structural misalignment driving classification delays, MOIT and MOST should transition Annex I away from broad HS codes and adopt a correlation matrix explicitly mapped to the Wassenaar Arrangement's Export Control Classification Numbers. Adopting the ECCN system would provide the technical granularity required to eliminate the over-capture of benign commercial goods, drastically reducing the number of false-positive license applications and relieving the administrative burden on both corporate engineers and state regulatory divisions.

While the mandate to integrate declarations into the VNSW portal represents a modernization effort, the dispersal of ultimate licensing authority across disparate bureaucracies risks bureaucratic siloing. Vietnam must ensure that the backend digital architecture of the Single Window operates via a unified risk-assessment engine. Cross-agency classification disputes regarding next-generation semiconductor equipment must be mediated swiftly by a standing, centralized, inter-agency task force possessing advanced technical expertise.

To prevent market consolidation triggered by high compliance costs from stifling domestic innovation, the state must also support smaller actors. MOIT, in coordination with the National Innovation Center, should provide subsidized compliance training programs and distribute open-source, state-approved end-user screening software to domestic semiconductor startups. By systematically lowering the internal time burdens and external consulting costs associated with navigating the SCM, the state can cultivate a diverse local ecosystem capable of integrating with global supply chains.

The long-term success of Vietnam's national semiconductor strategy hinges on institutional agility. By continuously refining the mechanical implementation of Decree 259 to minimize administrative burdens for compliant actors while maintaining strict prevention of illicit technology transfer, Vietnam can solidify its geopolitical and economic position as a trusted node in global semiconductor manufacturing.

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DOAN QUOC DZUNG is a seasoned development program and government relations expert with over a decade of experience in Vietnam and the broader Asia Pacific region. As the Program Strategy and Delivery Manager at Boston Consulting Group, he currently leads on-the-ground implementation of the Aus4Growth program, Australia's flagship economic development initiative in Vietnam. Dzung's career is marked by continuous works on translating policies into actions, having previously served as the Technical Pillar Director for the USAID Improving Private Sector Competitiveness project with Deloitte Consulting. His work has also included pioneering roles with the International Finance Corporation and the Mekong Institute, where he managed strategic initiatives focused on strengthening private sector innovation and promoting decarbonisation in manufacturing and agriculture sectors. As a Fulbright University alumnus with a master's in public policy, Dzung is a specialist in fostering public-private partnerships and navigating complex policy landscapes to drive impactful and sustainable change

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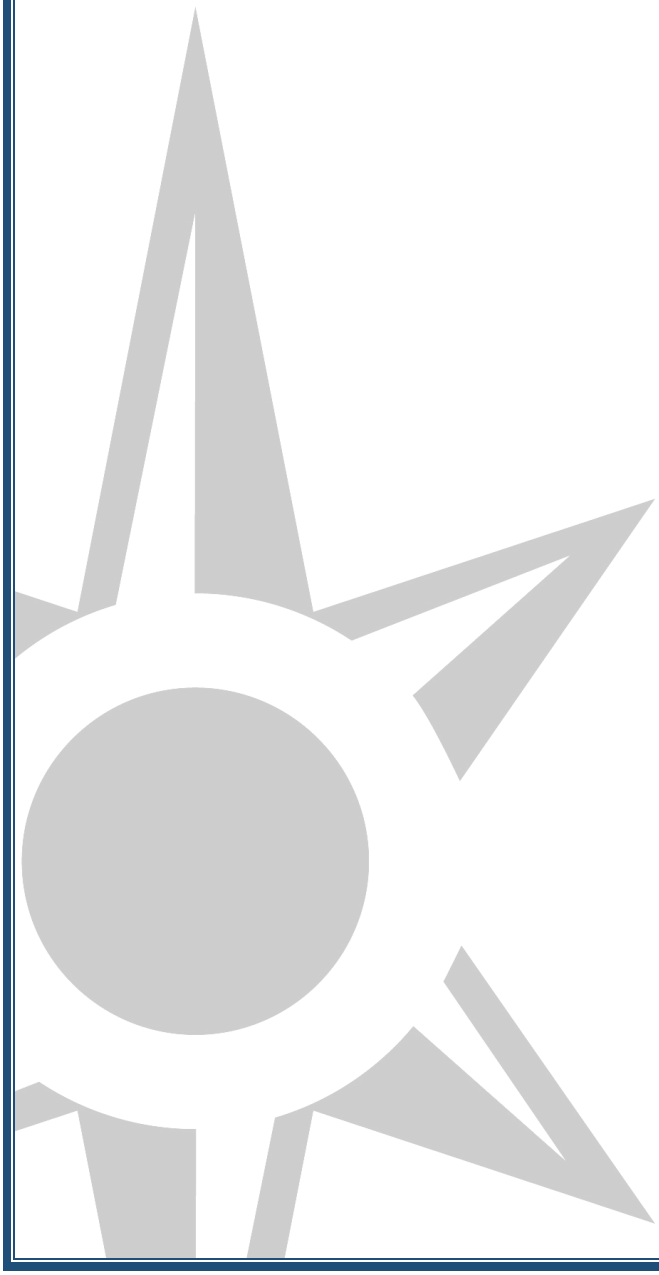
Building a Policy Framework to Foster Innovation and Investment in Vietnam's Semiconductor Industry: Insights from Da Nang City

By
Phuc Le



Executive Summary

Phuc Le

Vietnam has entered a decisive phase in its semiconductor strategy. The country has attracted major foreign investors, expanded chip design and assembly activity, and elevated semiconductors within its national development agenda. Yet the central policy challenge is not whether Vietnam can join the semiconductor value chain. It already has. The harder question is whether Vietnam can move from assembly-led participation toward an innovation-led role that creates domestic technological capability, trusted partnerships, and higher-value investment.

This paper argues that Vietnam should not pursue a broad, subsidy-heavy semiconductor strategy that imitates larger economies. Instead, it should build a targeted legal and policy framework suited to a latecomer economy: one that strengthens intellectual property protection without blocking learning, improves technology transfer rules, builds shared infrastructure, creates credible compliance mechanisms, and uses the Vietnam-US partnership to attract high-value investment in design, advanced packaging, materials, equipment services, and fabless ventures.

Vietnam is facing five constraints: First, the legal framework for semiconductors remains fragmented across intellectual property, technology transfer, investment, tax, customs, science and technology, education, and security-related rules. These laws point in a pro-innovation direction, but implementation remains uneven. Second, domestic firms and universities depend heavily on foreign electronic design automation tools, IP blocks, process know-how, and overseas foundries. This dependence becomes more sensitive as export controls and supply chain security rules reshape technology access. Third, Vietnam's talent base is growing but remains quite small and unevenly prepared for full-flow chip design, advanced packaging, process engineering, reliability testing, and technology commercialization. Fourth, foreign direct investment has not automatically produced strong domestic spillovers because many local firms lack the IP, capital, senior experts, prototyping infrastructure, and global customer access needed to absorb knowledge. Fifth, basic and advanced infrastructure – reliable power, clean water, logistics, cleanroom-ready parks, design centers, testing labs, and packaging pilots - remains uneven.

The paper recommends a practical framework built around public inputs and institutional capability rather than open-ended subsidies. Vietnam should establish cross-cutting enabling rules for semiconductor innovation, including clearer treatment of patents, trade secrets, layout designs, software, and university-generated IP. It should create a Semiconductor Innovation Fund that cofinances EDA access, MPW runs, packaging prototypes, reliability testing, and university spin-offs. It should clarify public-private research contracts and IP ownership, expand research and experimental-use flexibilities consistent with international rules, and build trusted licensing channels for foreign technology.

Enforcement matters as much as incentives. Vietnam should create specialized capacity for technology-related IP disputes, including trained judges, expert rosters, arbitration options, confidential evidence procedures, and stronger customs coordination. A high-level national semiconductor coordination body should lead overall policy, while the Ministry of Science and Technology should coordinate IP and innovation governance with the National Office of Intellectual Property, education, finance, customs, public security, courts, and local authorities.

Finally, Vietnam should use the Vietnam-US Comprehensive Strategic Partnership to move from diplomatic aspiration to project-level delivery. A bilateral semiconductor investment window could provide regulatory guidance, export-control compliance support, matchmaking, and fast-track facilitation for US firms and Vietnamese partners. Da Nang can serve as a controlled sandbox for shared labs, advanced packaging pilots, startup procurement, and university-industry collaboration. Such a strategy would help Vietnam become not

only a low-cost production site, but a trusted innovation partner in a more diversified Indo-Pacific semiconductor ecosystem.

I. Introduction

Semiconductors now sit at the intersection of economic development, technological competition, and national security. For Vietnam, this creates both opportunity and discipline. The opportunity is clear: global firms want more diversified supply chains, and Vietnam offers political stability, a young engineering workforce, proximity to Asian production networks, and improving relations with the United States and other technology partners. The discipline is equally clear: semiconductors are not a normal manufacturing sector. They require patient capital, specialized talent, trusted intellectual property (IP) rules, export-control awareness, reliable infrastructure, and institutions that can coordinate across ministries and markets.

This paper asks a practical policy question: how can Vietnam design a legal and policy framework that attracts high-value semiconductor investment while building domestic innovation capacity? The answer is not to copy the US CHIPS Act, Taiwan's foundry model, Korea's conglomerate-led model, or China's state-led subsidy model, etc. Vietnam has a smaller market, more limited fiscal space, and a semiconductor ecosystem still concentrated in foreign direct investment (FDI), design services, assembly, testing, and packaging. It therefore needs a selective framework that prioritizes public inputs, institutional credibility, and strategic partnerships.

A useful starting point is the World Bank's recent reframing of industrial policy. Rather than treating industrial policy as tariffs or subsidies alone, the World Bank defines it as government action to promote strategic business activities and stresses that governments with limited fiscal space should prioritize public inputs, capable institutions, skills, infrastructure, industrial parks, and quality systems before turning to costly incentives. This logic fits Vietnam's semiconductor challenge. The country should not try to win a global subsidy race. It should identify the bottlenecks that prevent firms, universities, and investors from learning, licensing, prototyping, and scaling.[1]

The paper advances three arguments. First, Vietnam's main challenge is not only attracting more semiconductor FDI but converting FDI into domestic capability. Second, IP and compliance rules should function as innovation infrastructure, not merely as legal protection. Third, the Vietnam-US partnership can accelerate investment and technology transfer only if Vietnam offers predictable rules, credible enforcement, and project-level facilitation.

Vietnam's Semiconductor Bottlenecks

Vietnam has already become part of the global semiconductor economy, but its role remains uneven. Its strongest current positions lie in assembly, testing, packaging, design services, and engineering support for multinational firms. These activities matter. They create jobs, expose Vietnamese engineers to global workflows, and help the country build trust with international partners. But they do not automatically create domestic product companies, proprietary IP, or advanced process capability.

The first bottleneck is regulatory fragmentation. Semiconductor projects touch IP law, technology transfer rules, investment incentives, customs procedures, tax administration, public procurement, education policy, cybersecurity, data protection, export-control compliance, and industrial land. Vietnam has adopted new strategies and laws that point toward a stronger innovation economy, but investors and startups still face uncertainty when moving from policy direction to implementation. A chip design startup may need EDA licenses, access to IP blocks, MPW financing, foreign foundry arrangements, data-security protocols, and tax treatment for R&D expenses. A packaging venture may need imported equipment, cleanroom permitting, reliability testing, customs facilitation, and trained technicians. If each issue sits in a separate administrative channel, speed and predictability suffer.

The second bottleneck is dependence on foreign technology platforms. Vietnam's semiconductor design ecosystem depends heavily on global EDA vendors, foreign IP libraries, offshore foundries, and imported equipment. This is normal for a latecomer economy, but it creates strategic vulnerability. Access to advanced design tools, high-performance computing chips, equipment, and certain process technologies can be affected by export controls, vendor risk assessments, and geopolitical rules. The

[1] World Bank, "Industrial Policy for Development: Approaches in the 21st Century" (Washington, DC: World Bank, 2026).

US and allied export-control measures since 2022 show that technology access increasingly depends on compliance credibility, end-use transparency, and trusted partnerships, not only commercial demand. Vietnam should treat this as a central policy issue rather than a secondary legal topic.[2]

The third bottleneck is talent. Vietnam has many engineering graduates, but semiconductors require specialized and experience-intensive capability. Recent reporting and policy discussions cite a national target of 50,000 semiconductor personnel by 2030, while current specialists remain far below that level. The issue is not only the number of graduates. Firms need engineers who can work across full design flows, packaging design rules, verification, validation, process integration, reliability, failure analysis, and product qualification. Universities need more faculty with industry experience, more licensed tools, more hands-on labs, and more industry-led curricula.[3]

The fourth bottleneck is weak domestic spillover from FDI. Foreign design centers and assembly plants can raise skills, but domestic firms will not automatically climb the value chain. Spillovers remain limited when local firms lack access to IP, senior technical mentors, prototyping funds, quality systems, and customers willing to qualify local suppliers. Many FDI centers operate as offshore engineering units or production subsidiaries serving parent-company roadmaps. Without deliberate linkage programs, domestic firms may remain service providers rather than product owners.

The fifth bottleneck is infrastructure, both basic and advanced. Semiconductor manufacturing and advanced packaging require reliable electricity, stable water supply, specialized waste treatment, logistics, customs predictability, and cleanroom-ready industrial zones. Design and startup ecosystems require less physical infrastructure than fabs, but they still need shared design centers, cloud and compute resources, secure data environments, MPW programs, packaging pilots, test equipment, and reliability labs. The Organization for Economic Co-operation and Development (OECD) similarly emphasizes that semiconductor resilience depends on skilled workers and robust infrastructure, including reliable energy, water, and transport systems.[4]

II. A Disciplined Industrial Policy for a Latecomer Economy

Industrial policy has returned to the center of semiconductor strategy, but Vietnam should use it selectively. Major economies deploy large subsidies because they seek domestic manufacturing capacity, national security resilience, and technological leadership. Vietnam's priority should be different: build public inputs that lower the cost of learning and make private investment more productive.

This means four policy shifts. First, Vietnam should prioritize shared infrastructure over broad subsidies. National or regional design centers can give universities and startups access to EDA tools, design libraries, verification environments, and MPW coordination. Advanced packaging pilots can help firms prototype system-in-package, fan-out, flip-chip, and reliability-testing solutions without immediately building full commercial factories. Testing and failure-analysis labs can support automotive, power, Internet of Things, and AI hardware firms. These assets should operate under transparent access rules, fee schedules, confidentiality protections, and industry advisory boards.

Second, Vietnam should create a Semiconductor Innovation Fund or Foundation. The fund should not become a general subsidy window. It should be a competitive, milestone-based instrument for early-stage chip design, advanced packaging, materials, testing, and semiconductor software. Eligible uses should include EDA seats, IP block evaluation, MPW runs, packaging prototypes, reliability testing, patent filing, and customer qualification. Support should require measurable outputs such as tape-outs, prototypes, licensing contracts, spin-offs, patents, or supplier qualification. Public money should reduce entry barriers, while private cofinancing should test commercial seriousness.

[2] US Department of Commerce, Bureau of Industry and Security, "Export Controls on Advanced Computing and Semiconductor Manufacturing Items," Oct. 7, 2022.

[3] World Bank, “Forging Viet Nam's Semiconductor Future: Talent and Innovation Leading the Way” (Washington, DC: World Bank, 2025).

[4] Organization for Economic Co-operation and Development, "Special Focus: Semiconductor Value Chains," Economic Security in a Changing World (Paris: OECD, 2025).

Third, Vietnam should use incentives to reward learning and linkage, not only capital expenditure. Tax incentives and land support can attract investors, but they should be tied to activities that build local capacity: training Vietnamese engineers, using local suppliers where feasible, funding university labs, licensing technology to domestic partners, or co-developing products with local firms. This approach reduces the risk that Vietnam competes only on labor cost.

Fourth, policy should identify realistic segments. A full advanced wafer fabrication strategy is expensive and risky. Vietnam can still move up the value chain through design services, fabless startups, embedded and application-specific chips, advanced packaging, testing, materials services, equipment maintenance, and secure supply-chain functions. These areas align better with Vietnam's existing capabilities and with global demand for supply chain diversification.

III. IP and technology transfer as innovation infrastructure

IP policy should support both protection and learning. Semiconductor innovation relies on patents, trade secrets, copyrighted software, layout designs, design libraries, process recipes, and confidential know-how. Investors will not transfer sensitive technology into a jurisdiction they do not trust. At the same time, an overly rigid IP environment can prevent universities, startups, and engineers from learning.

Vietnam should clarify the treatment of semiconductor-related assets under existing law. Integrated circuit layout designs already receive protection, but firms need clearer guidance on registration, originality, evidence, ownership, and commercialization. Patents should be examined rigorously for novelty, inventive step, and industrial applicability in device structures, packaging, manufacturing processes, and embedded systems. Trade secret rules should protect process recipes, yield data, reliability methods, customer specifications, and manufacturing know-how. Courts and administrative bodies should be able to protect confidential evidence during disputes.

The goal should be quality rather than quantity. Weak or overly broad patents can create barriers for follow-on innovation. High-quality examination and predictable enforcement make Vietnam more attractive to foreign partners while preserving space for domestic firms to improve, adapt, and commercialize.

Vietnam should also use flexibilities available under the Agreement on Trade-Related Aspects of Intellectual Property Rights (TRIPS). TRIPS establishes minimum standards, but it allows countries to design exceptions that support research and education, provided they do not unreasonably conflict with normal commercial exploitation. A clear experimental-use exception would allow universities and public research institutions to conduct noncommercial research, benchmarking, training, and proof-of-concept work. Carefully defined reverse-engineering allowances for interoperability and education can support learning without legalizing misappropriation.[5]

Technology transfer rules also need modernization. Semiconductor collaboration often uses hybrid models: joint development agreements, university spin-offs, IP-backed ventures, foundry access contracts, packaging process licenses, and customer-funded prototypes. Vietnam should create model clauses for IP ownership, background IP, foreground IP, confidentiality, export-control compliance, publication rights, revenue sharing, and dispute resolution. These templates would reduce transaction costs and reassure US and other foreign partners.

This is not necessarily a call for one standalone semiconductor law. A more practical approach is cross-cutting reform: implementing rules and amendments across IP, technology transfer, investment, customs, public R&D funding, data security, and competition law. Such a framework would help firms move from research to product without navigating inconsistent rules.

IV. Enforcement and Governance

Legal rights have little value without credible enforcement. For semiconductor investors, enforcement must be fast, technically informed, confidential, and coordinated. Vietnam's enforcement system should therefore evolve from

[5] World Trade Organization, "Agreement on Trade-Related Aspects of Intellectual Property Rights," April 15, 1994.

general IP administration toward strategic-technology enforcement capacity.

The first priority is specialized expertise. Patent, trade secret, and licensing disputes in semiconductors can involve circuit layouts, EDA files, process flows, packaging design rules, reliability data, and confidential customer specifications. Judges, prosecutors, customs officials, inspectors, and arbitrators need training in these technologies. Vietnam could establish dedicated IP chambers or high-technology panels within existing courts before creating a fully separate court. It could also develop expert rosters for semiconductor cases, with strict conflict-of-interest rules.

The second priority is confidentiality. Semiconductor disputes often require parties to submit sensitive technical documents. If courts or administrative agencies cannot protect confidential evidence, foreign firms will avoid local litigation and may hesitate to transfer technology. Vietnam should adopt protective orders, sealed evidence procedures, limited-access expert review, and penalties for unauthorized disclosure.

The third priority is arbitration. Many semiconductor contracts involve cross-border parties and confidential know-how. Vietnam should encourage specialized arbitration clauses for licensing, joint development, and technology transfer contracts. A high-tech arbitration roster would allow disputes to be resolved by arbitrators who understand IP, export controls, and semiconductor business models.

The fourth priority is border and supply-chain enforcement. Counterfeit components, unauthorized imports, and grey-market equipment can damage both safety and investor confidence. Customs authorities should receive semiconductor-specific training and digital tools to distinguish ordinary electronics trade from suspicious transfers involving restricted equipment, counterfeit chips, or infringing components.

Finally, enforcement must be coordinated. The Ministry of Science and Technology should coordinate IP and innovation policy with the National Office of Intellectual Property, the Ministry of Industry and Trade, the Ministry of Finance and customs authorities, the Ministry of Education and Training, the Ministry of Public Security, and the courts. Overall chip policy should sit under a high-level national semiconductor coordination body with authority to resolve cross-ministerial bottlenecks, monitor progress, and align national and provincial programs.

V. Leveraging Vietnam-US cooperation and Da Nang's sandbox role

The Vietnam-US Comprehensive Strategic Partnership gives Vietnam a rare opening to connect domestic reform with international investment. In 2023, the two countries elevated relations and announced cooperation on semiconductor supply chains, workforce, and ecosystem development, including initial US support for semiconductor training and ecosystem work in Vietnam. But diplomatic frameworks do not automatically produce technology transfer. Firms need project-level clarity.[6]

Vietnam should create a Vietnam-US semiconductor investment facilitation window. This would not be a political office. It should be a practical interface for companies, universities, investors, and provincial authorities. Its functions should include regulatory guidance, partner matchmaking, export-control compliance orientation, trusted end-use documentation, customs coordination, and referral to qualified labs, universities, and industrial zones. It should prioritize design centers, advanced packaging, EDA-related services, materials, equipment maintenance, secure electronics, and fabless ventures. The window should also support compliance with US and allied export-control expectations. Vietnam's advantage will grow if companies view it as a trusted, transparent, and rules-based partner. That requires clear procedures for end-use screening, restricted-party checks, data security, IP protection, and technology licensing. Compliance should not be treated as a barrier to investment; it should become part of Vietnam's value proposition.

Joint research and workforce programs should move beyond general training. Vietnam and US partners could develop advanced packaging curricula, chiplet design modules, reliability testing programs, secure hardware courses, and industry fellowships. Programs should include faculty training and lab access, not only student lectures. Vietnamese

[6] White House, "Fact Sheet: President Joseph R. Biden and General Secretary Nguyen Phu Trong Announce the US-Vietnam Comprehensive Strategic Partnership," Sept. 10, 2023.

engineers need exposure to real design flows, product qualification, and customer requirements.

Da Nang can pilot this model through a semiconductor regulatory sandbox. The city has experience in digital and semiconductor policy, a growing innovation ecosystem, and an emerging advanced packaging focus through VSAP Lab and related partners. A sandbox could test shared lab governance, fast-track startup support, university-industry IP templates, packaging prototype vouchers, and procurement mechanisms for domestic chip-related products. National authorities should supervise the sandbox, but local implementation would allow faster experimentation.

The key is to avoid a symbolic sandbox. It should have clear eligibility rules, measurable targets, confidentiality standards, compliance safeguards, and a pathway for scaling successful rules nationally. If designed well, Da Nang could become a testbed for how Vietnam links local capability building with trusted international semiconductor cooperation.

VI. Policy Roadmap

Vietnam should translate this framework into a small number of actionable reforms.

First, establish a national semiconductor coordination body with a mandate to align IP, investment, education, infrastructure, customs, and international cooperation. The body should publish annual progress indicators, including talent numbers, startup support, MPW participation, lab utilization, domestic supplier development, technology transfer agreements, and FDI linkage outcomes.

Second, create cross-cutting implementing rules for semiconductor IP and technology transfer. These rules should clarify ownership of publicly funded research, university spin-off rights, joint research contracts, trade secret protection, layout design registration, licensing templates, and experimental-use exceptions.

Third, launch a Semiconductor Innovation Fund with milestone-based grants and matching finance. The first funding windows should support EDA access, MPW runs, packaging prototypes, reliability testing, patent filings, and customer qualification.

Fourth, build shared infrastructure platforms. Vietnam should prioritize national design hubs, advanced packaging and testing pilots, reliability labs, and secure data environments before committing excessive resources to high-risk fabrication projects.

Fifth, strengthen enforcement capacity. Vietnam should train judges and enforcement officials, create expert rosters, adopt confidential evidence procedures, encourage high-tech arbitration, and improve customs monitoring of semiconductor-related goods and equipment.

Sixth, create a Vietnam-US semiconductor investment facilitation window that converts strategic partnership language into projects. This window should help US and Vietnamese partners navigate licensing, export-control compliance, customs, incentives, and research collaboration.

Finally, authorize Da Nang as a pilot sandbox for semiconductor innovation. The sandbox should focus on advanced packaging, chip design support, startup prototyping, university-industry collaboration, and trusted international partnerships. Lessons from Da Nang could then inform national policy.

VII. Conclusion

Vietnam has an opportunity to become a trusted semiconductor partner in the Indo-Pacific, but it will not succeed by relying only on low-cost labor, general incentives, or diplomatic momentum. The country must build the legal and institutional foundations that allow firms to innovate, protect technology, comply with international rules, and learn from global partners.

The most important shift is from attraction to absorption. Attracting FDI remains necessary, but Vietnam's long-term gains will depend on whether domestic firms, universities, and engineers can absorb knowledge and create proprietary value. That requires shared infrastructure, credible IP rules, capable enforcement, better university-industry linkages, and targeted finance for startups and prototypes.

A disciplined strategy would also strengthen Vietnam-US cooperation. US firms need trusted partners, secure supply chains, and predictable rules.

Vietnam needs technology, talent development, and higher-value investment. The overlap is real, but it requires implementation. A bilateral investment window and a Da Nang sandbox can help turn strategic alignment into projects.

Vietnam should therefore pursue a semiconductor policy that is ambitious but selective. It should avoid an unfocused subsidy race and instead invest in public inputs and institutions that make private innovation possible. If Vietnam gets these foundations right, it can move from assembly-led growth toward an innovation-led semiconductor role that supports national development and contributes to a more resilient Indo-Pacific technology ecosystem.

ABOUT THE AUTHOR

PHUC LE is the Director of the Da Nang Semiconductor & AI Center (DSAC), where he leads the city's strategy to build a competitive semiconductor and AI ecosystem. With 16 years of experience across the public sector, research, and teaching, he brings strong policy and innovation management expertise to advance Vietnam's deep-tech ambitions. At DSAC, Phuc drives talent pipelines, industry partnerships, and startup enablement with global partners such as NVIDIA, Synopsys, Google, and Arizona State University. His portfolio spans VLSI design training, an advanced packaging lab effort, AI/HPC infrastructure for sovereign capability, and policy facilitation to attract high-tech investment. He advises on AI and semiconductor policy and works closely with local and international stakeholders to accelerate technology transfer, commercialization, and market adoption across Vietnam and the broader region.

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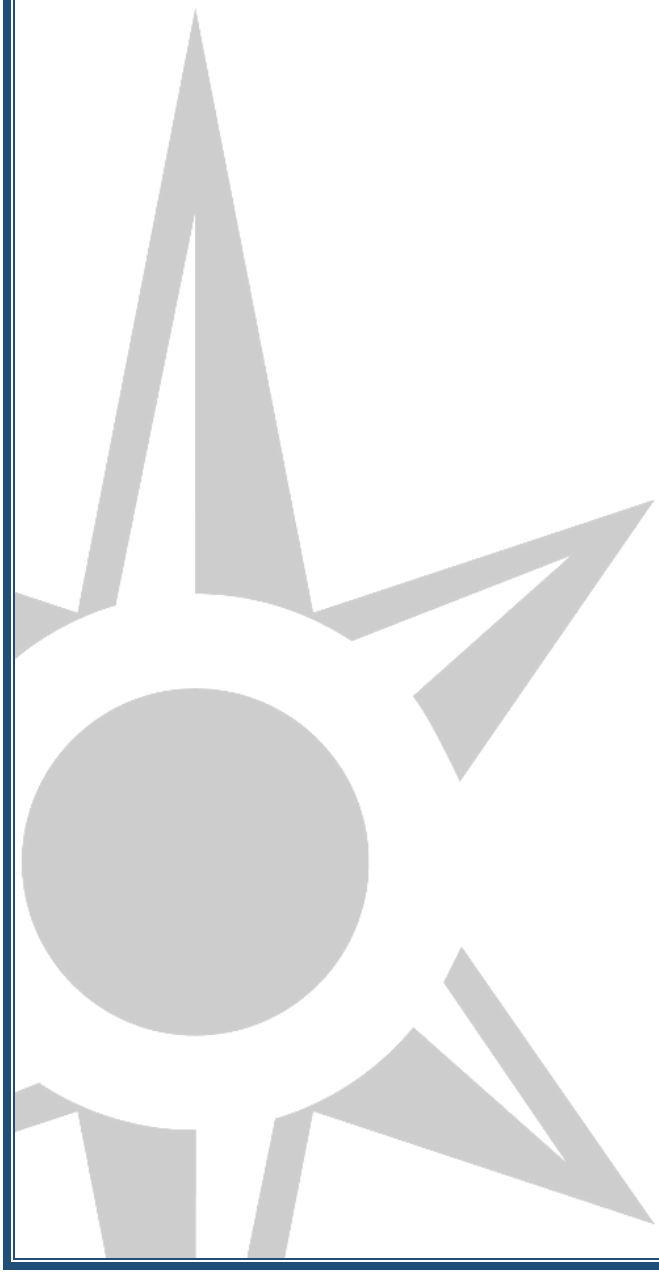
Building a Trusted Semiconductor Ecosystem in Vietnam:

Institutional Reform and US–Vietnam Partnership

By
Nguyen Quoc Cuong



Executive Summary

Nguyen Quoc Cuong

Vietnam's semiconductor ambitions are advancing amid supply-chain diversification, technology controls, and strategic competition. The country's most credible near-term opportunity is in assembly, testing, packaging, design services, and selected research partnerships, rather than immediate pursuit of capital-intensive leading-edge fabrication. Moving from a cost-competitive manufacturing location to a trusted node in security-sensitive semiconductor networks, however, requires more than industrial incentives. It requires institutions that reassure investors, partner governments, and customers that sensitive technology, data, and intellectual property will be protected and that compliance obligations will be implemented consistently.

This paper develops a policy framework for a trusted semiconductor ecosystem and applies it to Vietnam. The analysis combines a structured review of recent literature, policy and regulatory document analysis, comparative benchmarking against South Korea, Taiwan, and the United States, and synthesis of secondary indicators on investment, workforce, and market positioning. It also incorporates recent developments that materially alter Vietnam's policy landscape, including Decision No. 1017/QD-TTg on semiconductor human resources, Decision No. 1018/QD-TTg on semiconductor industry development, and Decree No. 259/2025/ND-CP on strategic trade control. These measures indicate that Vietnam is beginning to build not only industrial capacity, but also the legal and administrative foundations required for trust-based integration with US and allied supply chains.

The paper argues that Vietnam's competitive advantage will depend on aligning six dimensions: strategic trade controls and corporate compliance; governance of intangible technology transfer; intellectual property and trade-secret enforcement; cyber-physical security and supply-chain integrity; workforce and research capability; and infrastructure, sustainability, and operational reliability. It further argues that US-Vietnam semiconductor cooperation should be treated as an institution-building agenda, not only an investment agenda. The most valuable partnerships will be those that deepen compliance capability, create secure research and prototyping channels, upgrade talent pipelines, and establish auditable trusted-ATP pathways. The paper concludes with a phased reform and partnership roadmap for 2026-2030 and identifies future research priorities for fieldwork, firm-level compliance assessment, and ecosystem-assurance metrics.

I. Introduction

The semiconductor value chain is now a central arena of industrial competition, national security policy, and geoeconomic statecraft. Since the chip shortages of 2020-2022, governments and firms have moved away from a narrow efficiency model toward a resilience model in which concentration risk, export controls, logistics exposure, and alliance politics shape corporate strategy. Industry analysis suggests that new semiconductor sites are now assessed on sustainability, subsidy structure, and supply-chain security as much as on traditional cost variables [1]. Countries that wish to move into semiconductor production or services must therefore demonstrate not only cost competitiveness and labor availability, but also the institutional trust required to handle technology, equipment, process know-how, design IP, and sensitive customer data [2], [3], [4].

Vietnam has emerged as an increasingly visible candidate for this reconfiguration. Its broad electronics manufacturing base, political stability, improving logistics, and integration into regional and global trade agreements position it well to capture investment in assembly, testing, and packaging (ATP), design support, and selected research collaboration. Reuters has reported that Vietnam's share of the global ATP market could rise from about 1 percent in 2022 to 8-9 percent by 2032, a shift that would place the country in a materially stronger position within the back-end segment of the semiconductor value chain [5]. Major investments by Amkor, Intel, Hana Micron, Foxconn affiliates, and more recently Vietnamese players such as FPT suggest that Vietnam is no longer a speculative site on the semiconductor map; it is becoming an operational site with genuine scale [6], [7], [8], [9].

At the same time, Vietnam's policymakers are attempting to convert this momentum into a long-run national development strategy. Decision No. 1018/QD-TTg, issued on Sept. 21, 2024, sets out a phased roadmap for developing the semiconductor industry to 2030, with a vision to 2050. In its first phase, Vietnam seeks to build baseline capability across research, design, manufacturing, packaging, and testing; establish at least 100 design enterprises, one small-scale fabrication plant, and 10 packaging and testing plants; and train more than 50,000 engineers and bachelor's-degree holders by 2030 [10], [11]. On the same date, Decision No. 1017/QD-TTg approved a dedicated human resources program for the semiconductor industry through 2030, with the more detailed target of at least 50,000 university-level personnel, including at least 15,000 design engineers and at least 5,000 people with deep expertise in artificial intelligence [12], [13]. These decisions confirm that Vietnam views semiconductors not as a niche industrial activity, but as a strategic national capability.

A major new element is the evolution of Vietnam's trade-control architecture. In October 2025, the government promulgated Decree No. 259/2025/ND-CP on strategic trade control. The decree establishes a regulatory framework for dual-use goods and incorporates the concept of internal compliance programs (ICPs), including procedures for end-user review, legal updates, internal training, record

[1] McKinsey, "Exploring new regions: The greenfield opportunity in semiconductors," Jan. 29, 2024.
[2] Semiconductor Industry Association and Boston Consulting Group, "Emerging Resilience in the Semiconductor Supply Chain," 2024.
[3] US Government Accountability Office, "Policy Considerations from Selected Experts for Reducing Risks and Mitigating Shortages, GAO-22-105923," 2022.
[4] Center for Security and Emerging Technology, "The Semiconductor Supply Chain," Georgetown University, 2022.
[5] Reuters, "Vietnam expands chip packaging footprint as investors reduce China links," Nov. 12, 2024.
[6] Amkor Technology, "Amkor Inaugurates Latest Factory in Vietnam," Oct. 11, 2023.
[7] Intel, "Get to Know Intel Sites: Vietnam," 2024-2025.
[8] FPT Corporation, "FPT announces the establishment of an Advanced Semiconductor Testing and Packaging plant," Jan. 27-29, 2026.
[9] Reuters, "Foxconn subsidiary seeks $80 mln Vietnam investment for integrated circuits," Nov. 4, 2024.
[10] Prime Minister of Vietnam, Decision No. 1018/QD-TTg, "Strategy for development of Vietnam's semiconductor industry through 2030 and vision toward 2050," Sept. 21, 2024.
[11] Decision No. 1018/QD-TTg dated Sept. 21, 2024, Strategy for development of Vietnam's semiconductor industry through 2030, with a vision toward 2050.
[12] Ministry of Planning and Investment (Vietnam), "Human resources development programme for semiconductor industry approved," Sept. 21, 2024.
[13] Decision No. 1017/QD-TTg dated Sept. 21, 2024, Program on development of human resources for the semiconductor industry through 2030, with orientations toward 2050.

retention, and notification obligations [14]. For a country seeking deeper integration with US, Japanese, Korean, and Taiwanese supply chains, the decree is significant because it begins to institutionalize the language of compliance and controlled trade that increasingly governs advanced technology flows. It also strengthens the argument that the "trust challenge" in semiconductors is not only about IP law or cybersecurity. It is equally about whether firms and regulators can credibly manage sensitive items and knowledge in a way that aligns with international expectations.

The US-Vietnam Comprehensive Strategic Partnership, announced in September 2023, further raises the stakes. The partnership explicitly included a new semiconductor cooperation track and US support for semiconductor ecosystem and workforce development in Vietnam [15], [16]. This broader political framework intersects with the International Technology Security and Innovation (ITSI) Fund authorized by the US CHIPS and Science Act, under which the US Department of State works with partner countries on secure and trusted telecommunications and semiconductor supply chains [17], [18]. Through related efforts, including a 2024 Arizona State University-led workforce initiative supported by the State Department, the United States is already treating semiconductor cooperation with partner countries as an exercise in capacity-building and trust formation, not merely as commercial promotion [19].

The core question is therefore more specific than whether Vietnam can develop a semiconductor industry. The paper asks: how can Vietnam build a semiconductor ecosystem that is trusted for security-sensitive activities by investors, technology partners, and allied governments, while also serving Vietnam's long-term development and industrial upgrading goals? This framing matters because the future of semiconductor globalization is likely to be selective rather than universal. Not every location will host every segment of the value chain. Countries will compete for particular roles within trusted networks, and those roles will depend on the credibility of governance, compliance, and institutional capacity.

This paper makes four contributions. First, it offers an operational definition of a trusted semiconductor ecosystem that goes beyond generic references to resilience or investment attractiveness. Second, it updates the policy discussion by incorporating new legal and policy developments through early 2026, especially Vietnam's strategic trade control regime and human-resources agenda. Third, it draws on comparative insights from Pacific Forum's India Technology Policy Program and related policy literature to show that semiconductor ecosystem building requires an integrated policy stack linking talent, R&D, IP protection, compliance, and supply-chain security rather than a single investment lever [20]. Fourth, it proposes a phased reform and partnership roadmap for 2026-2030 aligned with Vietnam's national semiconductor strategy and US-linked cooperation mechanisms.

The remainder of the paper proceeds as follows. Section II reviews relevant scholarship and policy work on resilience, export controls, trusted technology ecosystems, and workforce development. Section III analyzes Vietnam's semiconductor landscape and explains why trust is emerging as the decisive constraint on moving up the value chain. Section IV explains the paper's methodology. Section V develops the trusted ecosystem framework. Section VI applies the framework to available evidence on market positioning, talent, compliance, and partnership instruments. Section VII discusses implementation risks and strategic trade-offs. Section VIII presents a phased policy reform and partnership roadmap. Section IX concludes and identifies future research priorities.

II. Related Work

The literature relevant to Vietnam's semiconductor ambitions spans four overlapping domains: supply-

[14] Government of Vietnam, Decree No. 259/2025/ND-CP on strategic trade control, Oct. 10, 2025.

[15] "Fact Sheet: President Joseph R. Biden and General Secretary Nguyen Phu Trong Announce the US-Vietnam Comprehensive Strategic Partnership," Sept. 10, 2023.

[16] Center for Strategic and International Studies, "An Indispensable Upgrade: The US-Vietnam Comprehensive Strategic Partnership," Aug. 19, 2024.

[17] "Congressional Research Service, CHIPS and Science Act of 2022: Semiconductors and the ITSI Fund," updated 2024-2025.

[18] Center for Strategic and International Studies, "Protect, Promote, Secure: Maximizing the ITSI Fund," May 15, 2023.

[19] Arizona State University, "Department of State and ASU announce new ITSI initiative," Feb. 20, 2024.

[20] Pacific Forum, Issues and Insights Vol. 25, SR 4, India Technology Policy Program Special Report, Sept. 2025.

chain resilience and industrial policy; strategic trade controls and technology security; ecosystem-building in late industrializers; and the governance of knowledge, talent, and trust in high-technology sectors. Taken together, these strands suggest that the transition from participation to trusted participation is the critical analytical shift for emerging semiconductor hubs.

The first domain examines supply chain resilience. Post-pandemic scholarship and policy analysis have documented how semiconductor production is geographically fragmented and highly concentrated at several chokepoints, including advanced fabrication, lithography equipment, specialty chemicals, electronic design automation (EDA), packaging expertise, and certain upstream materials [21]. The key insight is that resilience is not the same as autarky. Because no single country can efficiently control the entire semiconductor chain, resilience depends on diversification, redundancy, coordination among trusted partners, and visibility into weak points across the chain. This view is reinforced in policy reports by SIA-BCG, the US Government Accountability Office, CSET, and a growing number of comparative policy studies. For Vietnam, the implication is that the most realistic path is to become indispensable in selected niches while demonstrating dependable governance around those niches.

The second domain concerns export controls, strategic trade controls, and technology security. US and allied restrictions on advanced semiconductor equipment and high-end chips to China have shown that semiconductors are not governed solely by trade liberalization or industrial competitiveness. They are increasingly governed through security-minded administrative controls, end-use checks, investment screening, and research security measures [22]. In parallel, governments are paying greater attention to the risks of intangible technology transfer (ITT): the movement of controlled know-how through cloud access, software updates, technical assistance, engineering services, collaborative R&D, or academic exchange. This literature is directly relevant to Vietnam because trust in semiconductor supply chains increasingly depends on the ability of states, firms, and universities to govern knowledge flows, not just physical shipments. The issue is especially important in design support, validation, process engineering, and packaging, where proprietary knowledge may be embedded in service relations rather than in a visible physical good.

The third domain focuses on ecosystem-building and industrial upgrading in emerging economies. Comparative studies of Taiwan, South Korea, and the United States show that successful semiconductor ecosystems do not emerge from a single factory announcement. They depend on long-term institutional arrangements that connect state strategy, talent formation, research infrastructure, patient capital, and strong interfaces between universities and industry. Taiwan's experience highlights the importance of public research institutions and systematic technology transfer. South Korea's experience shows the role of coordinated industrial policy, scale, and national champions. The United States demonstrates the importance of design leadership, university research, venture capital, and later-stage industrial policy instruments such as the CHIPS Act. These cases differ in political economy, but they share one lesson: semiconductor capability is cumulative and institutionally embedded.

This lesson is strongly echoed in Pacific Forum's India Technology Policy Program papers. Across topics such as design incentives, IP protection, R&D policy, semiconductor law, and supply-chain security, those papers converge on the idea that industrial policy is insufficient if it is disconnected from trust-building institutions. In the India-focused papers, recurring themes include the need for stronger protection of design IP, integration of universities into talent development, more coherent trade-control architecture, and a better balance between production incentives and the support required for long-gestation design and R&D activities. The relevance for Vietnam is not that the two countries are identical. Rather, the India literature demonstrates that policy frameworks centered only on manufacturing targets often underinvest in the legal and institutional systems that determine whether firms will entrust sensitive knowledge and long-term projects to a new location.

[21] Zachary R.R. and Tho V.L., "Semiconductor supply chain resilience: Systematic review, conceptual framework, implementation challenges, and future research directions," Computers and Industrial Engineering, 2025.

[22] Megha S. and Amrita J., "China's semiconductor conundrum: understanding US export controls and their efficacy," Cogent Social Sciences, 2025.

The fourth domain centers on workforce and research ecosystems. For late entrants, the quality of talent pipelines often determines whether investment generates spillovers or remains enclave production. Vietnam already benefits from a strong electronics base, but multiple sources point to persistent shortages in advanced semiconductor design talent, packaging process engineers, faculty with semiconductor-specific expertise, and shared-use laboratory capacity [23], [24]. Recent Vietnamese policy documents recognize these constraints and move toward national solutions, including shared labs, specialized programs, and faculty training. Still, the literature suggests that quantitative targets alone are not enough. A trusted ecosystem requires talent that is not only technically capable, but also trained in compliance, data governance, quality management, and secure handling of proprietary information.

Another key strand in the literature addresses intellectual property, trade secrets, and ecosystem trust. In semiconductor activity, the most valuable assets are often invisible: process recipes, packaging flows, yield data, design libraries, test vectors, and software toolchains. Firms therefore evaluate locations not only on patent law in the abstract, but on the practical enforceability of trade secrets, the competence of judges and investigators, the speed of injunctive relief, and the security culture within counterpart organizations. This is where policy discussions increasingly overlap with cybersecurity. A fab, ATP line, or design center may be technically sound and commercially efficient, but if access controls are weak, insider risks are unmanaged, or supplier qualification is inconsistent, high-value projects may not materialize.

Vietnam-specific policy writing has begun to identify this intersection. Pacific Forum's 2024 blog on semiconductor supply and economic security in Vietnam argued that the country's partnership strategy with the United States, Japan, and South Korea should be understood as a means of strengthening economic security rather than simply attracting more foreign investment. That argument remains highly relevant. A trusted ecosystem is one in which external partners believe that investment in Vietnam reduces systemic risk rather than relocates it. This belief cannot be produced by branding alone; it must be supported by institutions, rules, and implementation capability.

At the same time, there are gaps in current literature. Much of the public discussion on Vietnam is still descriptive, emphasizing investment announcements and workforce targets without developing a fuller theory of trust. Some policy documents mention security but rarely specify the institutional levers through which trust can be measured or improved. There is also limited integration of strategic trade controls, ITT governance, IP enforcement, cyber-physical security, and workforce policy into a single analytical framework. This paper aims to address that gap by treating trust as a multi-dimensional governance challenge, not simply as an outcome of successful industrial promotion.

III. Vietnam's Semiconductor Landscape and the Trust Challenge

Vietnam's current semiconductor profile is strongest in the back-end and ecosystem-adjacent segments of the value chain. The country has become a major electronics manufacturing platform over the past two decades, anchored by large-scale production in consumer electronics, computing, communications equipment, and related components. This matters because semiconductor ATP activity and certain forms of subsystem manufacturing benefit from proximity to downstream electronics assembly, supplier networks, logistics infrastructure, and a workforce already familiar with electronics manufacturing disciplines. Vietnam's attractiveness therefore does not begin with semiconductors alone; it begins with the industrial base into which semiconductors can be embedded.

This base has helped attract major investments. Amkor inaugurated a major advanced packaging and test facility in Bac Ninh in 2023 and stated that the project would involve up to $1.6 billion over its first two phases. Intel's assembly and test facility in Ho Chi Minh City remains the largest ATP site in Intel's network, with cumulative official investment of roughly $1.5 billion. Reuters has reported that South Korea's Hana Micron plans to invest around 1.3 trillion won, or roughly $930 million, through 2026 to expand packaging operations in Vietnam. Foxconn's Shunsin subsidiary has pursued an integrated circuits board project in Bac Giang. Vietnam's sector scale is becoming more visible at the ecosystem level as well: by December 2024, Vietnam reportedly

[23] Pacific Forum, YL Blog #57, "Semiconductor Supply and Economic Security in Vietnam," Jan. 10, 2024.

[24] VOVWorld, "Human resource development crucial for Vietnam's semiconductor industry," Oct. 8, 2024.

hosted 174 foreign-invested semiconductor projects with nearly $11.6 billion in registered capital [25].

These developments are important for at least three reasons. First, they demonstrate that Vietnam has crossed from aspirational policy discourse into the phase of operational ecosystem building. Second, they indicate that global firms are increasingly willing to trust Vietnam with process-intensive, quality-sensitive production tasks that require stable infrastructure and large-scale labor management. Third, they create spillover opportunities in workforce development, supplier formation, and process learning. The presence of established multinational firms can help local universities and firms understand real demand conditions rather than training or investing in the abstract.

Yet Vietnam's landscape is still asymmetric. It is far stronger in manufacturing-adjacent services and ATP than in high-value original design, process R&D, advanced toolchain control, or domestic IP ownership. Pacific Forum observed in early 2024 that Vietnam's domestic design base was still narrow, centered on companies such as FPT and Viettel, while much of the higher-value activity was still closely tied to foreign-invested operations. Developments through 2025-2026 suggest that the domestic base is widening, but only gradually. The government has encouraged Viettel to develop semiconductor capabilities [26], while FPT in January 2026 announced the launch of the first fully Vietnamese-owned advanced semiconductor testing and packaging factory and framed the project as part of a broader push into sovereign capability, including design and AI-enabled applications. These are important signals, but they do not yet amount to a broad domestic innovation ecosystem.

This asymmetry creates the central trust challenge of Vietnam's semiconductor strategy. Moving from ATP and manufacturing spillovers into design collaboration, process co-development, advanced packaging for security-sensitive applications, or selective fabrication requires a deeper level of partner confidence. Firms and governments need to know not only that Vietnam can produce, but that it can protect. In practice, this means demonstrating credible control over four interrelated areas: strategic trade control and dual-use compliance; governance of intangible technology transfer; IP and trade-secret enforcement; and cyber-physical supply-chain security.

The first area is strategic trade control. As semiconductor supply chains become more entangled with export controls and end-use restrictions, investors increasingly examine whether a host country has clear control lists, predictable licensing processes, trained customs officials, and the administrative ability to distinguish ordinary trade from strategic trade. Vietnam's Decree No. 259/2025/ND-CP is thus a pivotal development. The decree introduces an institutional framework for managing dual-use goods and, importantly, encourages firms to establish internal compliance programs that include end-user review procedures, legal update procedures, internal training, recordkeeping, and notification obligations. This does not mean that Vietnam has solved the compliance problem. Rather, it means that the country has moved from a policy vacuum to a policy foundation. The next challenge is implementation: ICP certification, inter-agency coordination, sector-specific guidance, and the building of compliance culture inside firms and universities.

The second area is ITT governance. In emerging semiconductor hubs, this issue is often underappreciated because attention remains focused on physical equipment. But for design, packaging process engineering, yield optimization, or secure customer onboarding, much of the critical value is transmitted through software, service contracts, cloud platforms, remote debugging, data environments, or technical support. Vietnam's policy architecture still needs stronger, institution-level guidance on when such transfers may trigger strategic sensitivity, contractual risk, or trade-control obligations. Universities and research institutes in particular need practical protocols for research security, collaborator review, data access, and sponsored project governance. Without these, Vietnam may attract some investment while still failing to qualify for the most sensitive work packages.

The third area is IP protection and trade-secret enforcement. Vietnam has continued to improve its legal framework through trade agreements and domestic reform, but semiconductor-related trust depends on practical enforcement capacity rather

[25] VietnamPlus, "Vietnam home to 174 FDI projects in semiconductor sector," Dec. 16-17, 2024.

[26] Reuters, "Vietnam's Viettel to develop semiconductor industry, prime minister says," April 10, 2024.

than formal legal availability alone. Firms care about whether specialized expertise exists in courts or enforcement bodies, whether evidence can be preserved, whether interim remedies are timely, and whether insider-related misappropriation can be investigated effectively. This matters not only for chip design, but for packaging flows, reliability data, firmware, and testing procedures. The more Vietnam seeks to attract higher-value or defense-adjacent semiconductor work, the more this issue will move from a background concern to a first-order due diligence question.

The fourth area is cyber-physical security. Semiconductor ecosystems sit at the intersection of operational technology, IT systems, supplier management, and human access control. Vulnerabilities can arise from insecure data exchange, insufficient segmentation between enterprise and production systems, counterfeit or poorly qualified inputs, weak visitor controls, inadequate logging, or poor incident response. Because advanced packaging and test work can involve customer-owned IP and stringent quality regimes, Vietnam's move into trusted ATP will increasingly require auditable security practices across industrial parks, secure labs, and critical suppliers. In other words, the trust challenge is not confined to ministries or customs offices; it is embedded in the day-to-day operation of sites and counterpart organizations.

Comparative experience helps clarify Vietnam's path. Taiwan and South Korea built trust not only through industrial scale, but through dense ecosystems of institutions, engineers, suppliers, and specialized regulators. The United States remains central not only because of its design leadership, but because of the depth of its research, legal, compliance, and corporate governance systems. Vietnam cannot replicate these systems quickly or wholesale, but it can identify the institutional minimums required to become a credible node in trusted supply chains. This is precisely why policy debates should avoid a false choice between competitiveness and security. In semiconductors, particularly after 2020, the most competitive locations in sensitive segments are often those that can demonstrate security, compliance, and predictability as part of their value proposition.

Vietnam's trust challenge is therefore best understood as an upgrading challenge. The country has already shown that it can host globally significant back-end operations. The next stage is to convert industrial momentum into institutional depth. That conversion will determine whether Vietnam remains primarily an efficient manufacturing destination or becomes a genuinely trusted partner for higher-value semiconductor activities.

IV. Methodology

This paper adopts a qualitative case-study design supported by structured document review, comparative benchmarking, and secondary indicator analysis. The choice of methodology reflects the current state of Vietnam's semiconductor ecosystem: the sector is evolving rapidly, many policy measures are newly announced or only partially implemented, and comparable datasets remain fragmented across official documents, industry reports, news coverage, and policy analysis. Under these conditions, a mixed qualitative strategy is more appropriate than a narrow econometric approach because it allows the paper to integrate institutional, legal, and strategic dimensions that are often omitted from purely market-oriented accounts.

A. Structured Literature Review

The literature review focused on work published primarily between 2018 and early 2026 on semiconductor ecosystem development, supply-chain resilience, export controls, technology security, workforce policy, and IP governance. Sources were selected according to four criteria: relevance to semiconductors or semiconductor-adjacent governance; publication by peer-reviewed venues, government bodies, reputable think tanks, or industry associations; analytical value for emerging economies or partner-country cooperation; and applicability to Vietnam's institutional setting. The review included academic articles, policy papers, official strategy documents, industry studies, and carefully sourced media reports used mainly for investment and market updates.

The review was not intended to produce an exhaustive bibliometric inventory. Instead, it was designed to identify recurring analytical mechanisms: concentration risk, diversification logic, talent bottlenecks, compliance capacity, trust-based partnership models, and the institutional requirements for handling sensitive technology. Special attention was paid to policy-oriented work from Pacific Forum's India Technology Policy Program because those papers offer a rich set of

arguments on talent, R&D, IP, law, export controls, and ecosystem coherence that are highly relevant to Vietnam's current stage of development.

B. Policy and Regulatory Document Analysis

The paper relies heavily on official policy and regulatory documents because the argument centers on trust as an institutional and governance issue. Three Vietnamese instruments are especially important: Decision No. 1017/QD-TTg on human resources development for the semiconductor industry, Decision No. 1018/QD-TTg on the semiconductor industry development strategy, and Decree No. 259/2025/ND-CP on strategic trade control. Together, these instruments reveal how Vietnam is linking industrial ambition to workforce formation and, increasingly, to strategic trade governance.

On the US side, the paper examines documents related to the US-Vietnam Comprehensive Strategic Partnership, the ITSI Fund, and associated capacity-building initiatives. These sources are used not only to describe available instruments, but also to infer the types of governance capabilities that US and allied partners are likely to value in prospective semiconductor locations. The analysis therefore treats policy texts as signals of strategic intent, administrative priorities, and areas where partner expectations may shape ecosystem design.

C. Comparative Benchmarking

Comparative benchmarking is used to derive practical lessons rather than to rank ecosystems. South Korea, Taiwan, and the United States were chosen because each provides a distinct model of semiconductor capability. Taiwan illustrates the role of public R&D institutions, state-industry coordination, and specialization in foundry and packaging ecosystems. South Korea offers lessons on national champions, scale, and policy persistence. The United States demonstrates the combination of design leadership, university research, venture capital, standards influence, and recent industrial-policy resurgence through the CHIPS Act. These cases differ in size and political economy from Vietnam, but they provide reference points for understanding what kinds of institutions make trust credible in mature ecosystems.

The benchmarking framework centers on policy instruments that directly support trusted participation: export control and compliance architecture; institutional treatment of intangible technology transfer; IP and trade-secret enforcement; secure research environments; workforce mechanisms; and ecosystem assurance practices. The objective is not to recommend identical transplantation. Rather, it is to identify adaptable institutional functions that Vietnam could implement in scaled and context-appropriate form.

D. Conceptual Prototype for Future Fieldwork

A comprehensive assessment of ecosystem trust will ultimately require fieldwork involving stakeholder interviews and perception analysis. To support this objective, we introduce a conceptual prototype to illustrate how future fieldwork can operationalize the concept of trust. The demonstration uses a clearly labeled synthetic dataset based on ten trust-related variables grouped around regulatory confidence, ecosystem capability, infrastructure reliability, and research collaboration. The purpose here is strictly methodological: it shows how future field surveys could be analyzed through exploratory factor analysis to separate perceived gaps in regulatory trust from perceived gaps in ecosystem capability. This illustrative model should not be interpreted as empirical evidence of stakeholder preferences or as a substitute for actual interviews. Its value lies solely in clarifying the measurement logic of trust.

This demonstration should not be interpreted as proof of stakeholder preferences or as a substitute for actual interviews. Its value lies in clarifying measurement logic. Trust in semiconductor ecosystems is often discussed at a high level, but future empirical work will need to test whether stakeholders actually prioritize export-control capacity, ITT governance, trade-secret enforcement, cyber readiness, infrastructure stability, or talent availability differently across firm types and partner countries. By laying out a prototype analytics approach, the paper creates a bridge between conceptual work and future field research.

The methodology has three limitations. First, the paper depends on publicly available sources and therefore cannot fully capture firm-level due diligence criteria or confidential compliance concerns. Second, some investment figures are drawn from official announcements or media reports and should

be understood as indicative rather than as audited realized expenditure. Third, because much of Vietnam's trust architecture is still emerging, the paper necessarily analyzes both current capacity and policy trajectory. This limitation is unavoidable, but it is also analytically useful because trust in this sector is built prospectively: firms make location decisions based on both present capability and expected institutional direction.

V. Trusted Semiconductor Ecosystem Framework

This paper defines a trusted semiconductor ecosystem as an institutional and industrial configuration in which firms, investors, regulators, and partner governments can reasonably assess that sensitive semiconductor technologies, knowledge assets, and supply-chain relationships will be handled in a secure, predictable, and norm-consistent manner. Four elements are embedded in this definition. First, trust is not reducible to political alignment; it must be operationalized through institutions and practices. Second, trust must extend to both physical and intangible assets. Third, trust is relational: it depends on how external partners perceive risk in working with firms and institutions located in Vietnam. Fourth, trust is cumulative and auditable: it grows through repeated compliance, transparent governance, and credible remedies when problems arise.

Table 1. Operational dimensions of a trusted semiconductor ecosystem

Dimension	What trust requires	Illustrative levers	Near-term focus for Vietnam
Strategic trade controls and compliance	Clear control lists, licensing workflows, end-use checks, internal compliance culture, and enforceable procedures	Strategic trade control law; ICPs; customs and licensing modernization	Operationalize Decree 259/2025 and pilot ICP certification
Intangible technology transfer governance	Rules for handling know-how transfers through software, services, cloud access, and research collaboration	Research security guidance; ITT risk assessment; secure collaboration protocols	University and lab guidance for sponsored projects and remote engineering access
IP and trade secret enforcement	Predictable remedies, technical expertise, and deterrence for patent and trade secret violations	Specialized dockets; evidence handling; enforcement coordination	Faster handling of semiconductor-related disputes and stronger trade-secret practice
Cyber-physical security and integrity	Secure facilities, controlled data environments, incident response, and supplier integrity	Security audits; access controls; traceability; trusted supplier qualification	Trusted-ATP baseline standards for parks, labs, and critical suppliers
Talent and research capacity	Sustained pipelines of design, ATP, process, and compliance-aware professionals	Shared labs; joint curricula; scholarships; apprenticeships	Implement Decisions 1017/1018 through a national semiconductor education consortium
Infrastructure and operational reliability	Stable power, water, land readiness, ESG compliance, and continuity planning	Resilient utilities; green power options; transparent incentives	Target high-tech zones and anchor provinces for assured semiconductor infrastructure

To make the concept operational, the paper structures trust into six dimensions. Each dimension corresponds to a distinct policy domain but also interacts with the others. Table 1 summarizes the framework and the main policy levers associated

with each dimension. The framework is intended to help policymakers and ecosystem participants identify where bottlenecks are likely to occur as Vietnam seeks to move into higher-value semiconductor work.

The first dimension is Strategic Trade Controls and Compliance. At minimum, trust requires a clear legal basis for controlling sensitive items, administratively workable licensing procedures, the ability to identify end users and end uses, mechanisms for corporate compliance, and a credible enforcement backstop. In emerging semiconductor hubs, this dimension is often evaluated by external partners before they are willing to relocate sensitive equipment, process technology, or customer-specific production flows. Vietnam's Decree No. 259/2025/ND-CP is therefore foundational because it introduces a national framework for strategic trade goods and explicitly recognizes internal compliance programs. Yet a decree is only the first layer. Trust will ultimately depend on implementation details: whether control lists are understandable; whether licensing is timely and coordinated; whether customs and sectoral regulators have technical expertise; and whether firms establish real internal compliance structures rather than paper programs.

The second dimension is Governance of Intangible Technology Transfer. Semiconductors involve large volumes of know-how moving through design software, technical support, cloud platforms, simulation environments, firmware, and collaborative engineering. A trusted ecosystem needs processes for reviewing sensitive cross-border projects, securing design data, controlling access to EDA environments, and governing research partnerships with foreign entities. Universities, startups, ATP sites, and foreign-invested enterprises all face this issue in different ways. In practice, ITT governance includes contract design, information classification, secure collaboration platforms, institutional review procedures, and staff training on what constitutes a sensitive transfer. Weaknesses in this dimension can undermine otherwise strong physical trade controls because critical knowledge may move through service relations rather than through export shipments.

The third dimension is Intellectual Property Protection and Enforcement. Semiconductor ecosystems are built on a mix of patents, trade secrets, mask works, process know-how, proprietary testing flows, and customer-specific data. Trust in Vietnam as a location for higher-value activity therefore requires confidence that rights can be protected and that violations will be addressed quickly and competently. This means more than statutory compliance with international agreements. It means specialized knowledge in courts or adjudicative units, effective civil and criminal remedies where appropriate, reliable evidence handling, and practical coordination among police, customs, inspectors, and prosecutors. For emerging ecosystems, visible enforcement in a few well-handled cases may matter as much as the formal legal framework because firms infer the seriousness of the host environment from enforcement behavior.

The fourth dimension is Cyber-Physical Security and Supply-Chain Integrity. Semiconductor production and design are vulnerable to both digital and physical compromise. The ecosystem therefore requires strong access control, network segmentation, secure data environments, OT security, incident response capacity, traceability of inputs, supplier qualification, and counterfeit mitigation. For ATP sites in particular, trust depends on whether process data, testing environments, and customer material can be segregated and protected. As Vietnam moves toward more advanced packaging and design-linked services, this dimension will become more visible. Trusted-ATP status, in other words, will depend on secure production culture as much as on output volume.

The fifth dimension is Talent and Research Capacity. Semiconductor ecosystems are sustained by engineers, technicians, process specialists, faculty, lab managers, and compliance-aware managers who can translate strategy into execution. Trust enters here in two ways. First, external partners evaluate whether Vietnam can supply not just labor, but labor capable of handling advanced and sensitive work. Second, research institutions and university programs need to become reliable counterparts for joint training, prototyping, and co-development. Vietnam's Decisions No. 1017 and No. 1018 recognize this challenge by setting ambitious workforce and shared-laboratory goals. The critical issue is converting numerical targets into quality-assured pipelines through curricula, labs, faculty development, apprenticeships, and sustained industry engagement.

The sixth dimension is Infrastructure, Sustainability, and Operational Reliability. Semiconductor activity is highly sensitive to power quality, water reliability, logistics, land readiness, environmental compliance, and continuity planning. ESG expectations are also becoming more significant, especially for multinational customers and investors subject to corporate reporting requirements. For Vietnam, this dimension is not merely supportive; it is part of the trust proposition. A location that is cost-effective but exposed to recurrent infrastructure interruptions, opaque permitting, or sustainability risks may be acceptable for some low-value operations but not for high-value and security-sensitive projects.

These six dimensions are mutually reinforcing. A country may offer good infrastructure and an abundant workforce, but still fail to attract high-trust projects if its compliance or IP systems are weak. Conversely, strong legal commitments may be insufficient if firms cannot find trained staff or reliable utilities. The framework is therefore intentionally holistic. It invites policymakers to shift from a single-variable model of semiconductor development - such as incentives, factories, or workforce counts - to a systems model in which trust emerges from alignment across multiple institutions.

The framework also supports staged policy design. Not every dimension must reach frontier level before Vietnam can deepen its role in the global ecosystem. But each dimension should reach a threshold appropriate to the segment Vietnam wishes to host. For example, a basic ATP site may require different assurance standards from a site handling sensitive defense-adjacent chips or customer-specific advanced packaging. Similarly, a university involved in open semiconductor curriculum development faces different risks from a lab handling export-sensitive process knowledge. The policy implication is that Vietnam should build a modular assurance architecture: a core national baseline plus stricter protocols for higher-risk segments and actors.

Finally, the framework helps distinguish trusted participation from trusted branding. Many countries now present themselves as friend-shoring destinations. But in semiconductors, branding is not enough. Trust is earned when firms can verify compliance systems, observe enforcement behavior, see high-quality talent coming through the pipeline, and believe that their IP and sensitive know-how will be treated responsibly. The sections that follow apply this framework to Vietnam's current trajectory and the most relevant partnership instruments.

VI. Results

A. Market Positioning and Investment Signals

Vietnam's current market positioning is strongest in the backend of the semiconductor value chain and in adjacent electronics manufacturing activities. This positioning is not incidental. It reflects the country's accumulated strengths in labor-intensive yet quality-sensitive manufacturing, its participation in electronics export chains, and its ability to absorb large foreign-invested industrial projects. In that sense, Vietnam's semiconductor role is emerging from an existing industrial ecosystem rather than from a greenfield vacuum.

Available public indicators support the view that Vietnam is becoming a serious ATP location. Reuters reported in late 2024 that Vietnam could expand its share of global ATP capacity from roughly 1 percent in 2022 to 8-9 percent by 2032. Although any long-range forecast should be treated cautiously, the direction of travel is credible given ongoing project announcements and the broader strategic push by firms to diversify away from excessive reliance on China. Vietnam's geography, labor pool, and policy attention all strengthen this outlook.

Firm-level investments reinforce that picture. Amkor's Bac Ninh project signals confidence from a major global packaging and test firm in Vietnam as a long-horizon advanced packaging site. Intel's long-established and large-scale assembly and test presence provides Vietnam with deep operational learning and symbolic validation. Hana Micron's expansion indicates South Korean confidence in Vietnam's packaging prospects. Foxconn-linked activity shows that ecosystem-adjacent semiconductor and substrate-related projects are also entering the pipeline. Most importantly from a national-development perspective, FPT's 2026 launch of a fully Vietnamese-owned advanced semiconductor testing and packaging factory suggests that domestic firms are starting to move from software and system integration into more physical segments of the semiconductor chain.

Table 2. Selected investment signals in Vietnam's semiconductor-related ecosystem

Project	Status	Investment (USD bn)	Strategic implication
Amkor Bac Ninh advanced packaging and test	Operational since 2023	1.60	Anchors Vietnam in advanced back-end manufacturing and training-intensive packaging operations
Intel Products Vietnam ATP	Operational; cumulative investment	1.50	Validates Vietnam as a large-scale, high-reliability ATP location in a major global network
Hana Micron Bac Giang expansion	Planned through 2026	0.93	Deepens South Korean packaging footprint and expands back-end ecosystem scale
Foxconn / Shunsin IC boards facility	Planned	0.08	Adds ecosystem-adjacent electronics and substrate-related capability in northern Vietnam
FPT advanced semiconductor testing and packaging plant	Announced in 2026	N/A	Strengthens domestic participation and signals movement toward a more nationally embedded ecosystem

These developments, summarized in Table 2, matter strategically because ATP is no longer a low-trust residual segment. Advanced packaging is becoming a much more technologically significant stage of the value chain as chiplet architectures, heterogeneous integration, and system-level performance considerations grow in importance. That means the governance demands on ATP sites are rising as well. High-value ATP increasingly involves close interaction with sensitive customer designs, strict process controls, and proprietary reliability data. Vietnam's ability to capture this opportunity will therefore depend on whether it can pair scale with credible assurance.

A second important result concerns ecosystem breadth. VietnamPlus reported in December 2024 that Vietnam hosted 174 foreign-invested semiconductor projects with registered capital of nearly $11.6 billion. Even allowing for variation in project type and realization pace, this number suggests that the country is not building a single-site semiconductor story. It is building a distributed ecosystem involving industrial parks, universities, suppliers, equipment and materials interfaces, and multiple localities. This broadening matters because ecosystems become more resilient and attractive when firms can source services, recruit staff, and coordinate with other capable actors locally.

At the same time, the data also reveal a developmental imbalance. Much of the visible capital is still foreign and back-end oriented. Vietnam's immediate challenge is not to replace this model, which has delivered real gains, but to use it as a platform for capability deepening. That requires stronger domestic participation in design, validation, software-tool usage, testing IP, process engineering, secure supplier services, and eventually more research-linked segments. In short, Vietnam's market signal is positive, but its upgrading challenge remains unresolved.

B. Workforce Gap and Talent Pipeline

Workforce remains the binding constraint on Vietnam's long-term semiconductor strategy. Public policy now recognizes this clearly. Decision No. 1017/QD-TTg set a target of at least 50,000 university-level semiconductor personnel by 2030, including at least 42,000 engineers and bachelor's-level workers, 7,500 master's students, and 500 doctoral students; at least 15,000 are expected to work in design and at least 5,000 to possess deep AI expertise. Decision No. 1018 reinforces the headline target of more than 50,000 engineers and bachelor's-degree holders by 2030. These are large numbers relative to Vietnam's current baseline and show that workforce policy is now central, not peripheral, to industrial policy.

The scale of the challenge becomes clearer when set against current estimates. Figure 1 illustrates a simple baseline-to-target trajectory that helps visualize the annual expansion challenge implied by current policy goals. Public reporting in 2024 placed Vietnam's base of integrated-circuit or semiconductor engineers at roughly 5,570 to 6,000 people. A simple linear path from a 2023 baseline of 5,570 to 50,000 in 2030 implies net additions of roughly 6,300 trained personnel per year. Real-world scaling will not be linear, of course. The first years require expansion of faculty, lab infrastructure, curricula, scholarship support, and industry placements. But the arithmetic is still instructive: Vietnam must move from a relatively narrow talent base to a national pipeline of much greater scale within a compressed time frame.

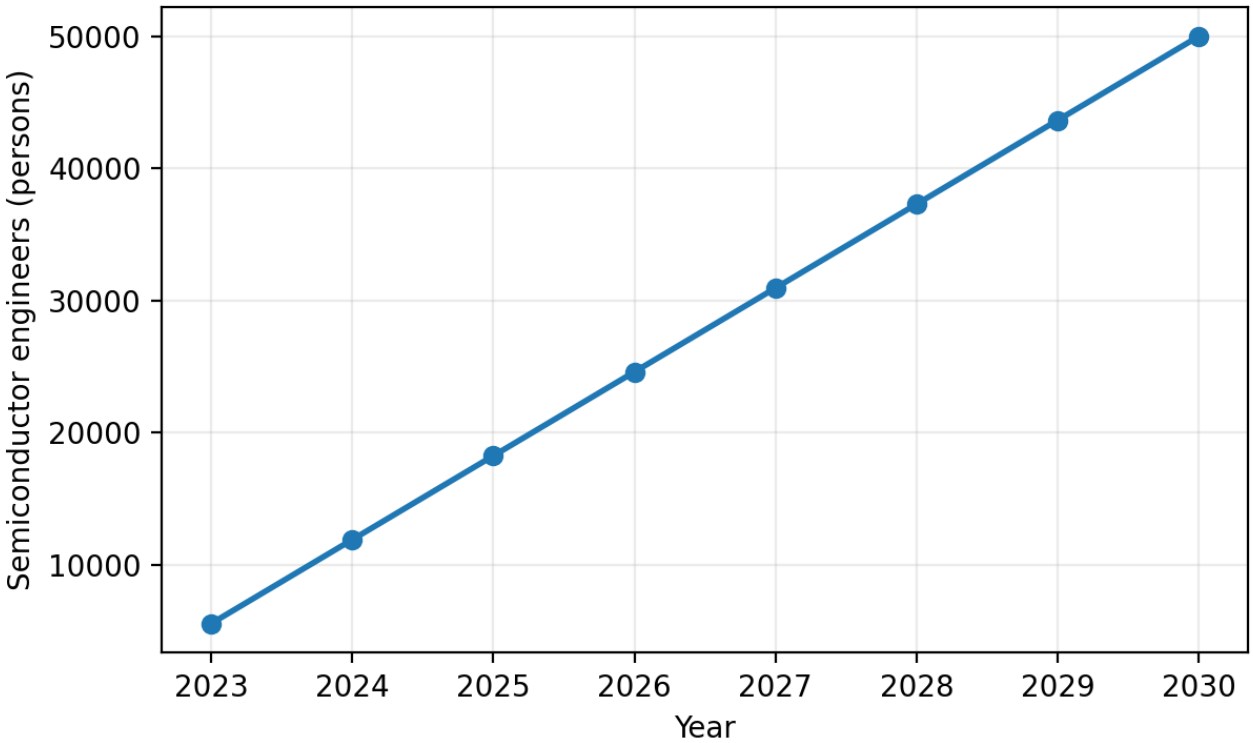


Figure 1. Illustrative workforce expansion trajectory toward 50,000 semiconductor personnel by 2030

The constraint is also qualitative. Semiconductor education is not interchangeable with general engineering education. Design engineers need experience with architectures, verification, EDA tools, and system constraints. ATP engineers require familiarity with packaging processes, yield management, reliability testing, materials interfaces, and equipment-intensive manufacturing discipline. Faculty and lab managers require a different type of capacity again. As a result, workforce development must be treated as a system involving universities, shared labs, scholarships, industry co-development, and sustained practical training.

There are encouraging signs. The human resources program approved in 2024 explicitly calls for investment in shared-use semiconductor laboratories and faculty development. FPT has announced a target of training 10,000 semiconductor engineers by 2030 as part of its ecosystem push. US-supported initiatives tied to the Comprehensive Strategic Partnership and the ITSI-related workforce agenda also provide openings for joint curriculum development, lab cooperation, and secure research training. However, these initiatives will only reach systemic scale if they are coordinated under a national architecture that links target-setting to institutional delivery.

The workforce result is therefore mixed but actionable. Vietnam has moved from vague aspiration to quantified planning, which is an important governance advance. Yet the distance between target and baseline remains large. The critical policy task is not merely to expand enrollment, but to create a trusted talent pipeline - one that combines technical depth, quality management, and the compliance awareness required in sensitive technology sectors.

C. Trust Gaps: Compliance, ITT, and IP Enforcement

The most consequential finding of this paper is that Vietnam's trust gap is no longer a single legal issue, such as IP protection, nor a single industrial issue, such as skill shortages. It is a composite governance gap spread across compliance, intangible technology transfer, and enforceable protection of proprietary knowledge. This gap does not negate Vietnam's progress. Instead, it explains why moving from ATP expansion to higher-value trusted participation remains difficult.

The strategic trade control picture has improved materially with Decree No. 259/2025/ND-CP. The decree is significant because it creates a legal basis for managing dual-use goods and formalizes the logic of internal compliance programs. However, Vietnam now faces the classic implementation challenge. From the perspective of private investors, the compliance burden is highly tangible. Global corporations operating large-scale ATP facilities, such as Amkor, Intel, and Hana Micron, as well as emerging domestic players like FPT, urgently need more than general investment incentives. To attract advanced packaging workflows containing proprietary customer data or sensitive technology, these facilities must demonstrate strict adherence to Internal Compliance Programs (ICPs). Yet, firms and research organizations currently lack practical, sector-specific protocols to assess foreign partners, classify sensitive technical data, or manage Intangible Technology Transfer (ITT) across cloud platforms. Investors require specific, operational guidance rather than just a broad regulatory umbrella.

ITT governance is therefore the next institutional frontier. Many organizations in emerging ecosystems lack routines for classifying sensitive technical information, reviewing foreign collaborators, or assessing whether cloud-based engineering access and service support create controlled-transfer risk. Without such routines, Vietnamese institutions may create vulnerabilities even while complying with physical export rules. In a field where design, simulation, testing, and process optimization increasingly involve remote collaboration, ITT governance should be treated as a core national capability rather than a secondary compliance issue.

IP and trade-secret enforcement present a similar pattern. Vietnam has improved legal alignment through trade agreements and domestic reform, but ecosystem trust depends on whether firms believe that remedies are practical, technically informed, and timely. In semiconductor work, the most commercially important assets are often difficult to observe and difficult to value: packaging recipes, testing methodologies, source code, design libraries, process windows, and customer qualification data. If firms fear that such assets cannot be protected effectively, they may limit what work is transferred to Vietnam or retain the highest-value segments elsewhere. Strengthening specialized adjudication, evidence handling, trade-secret practice, and visible enforcement would therefore have outsized signaling value.

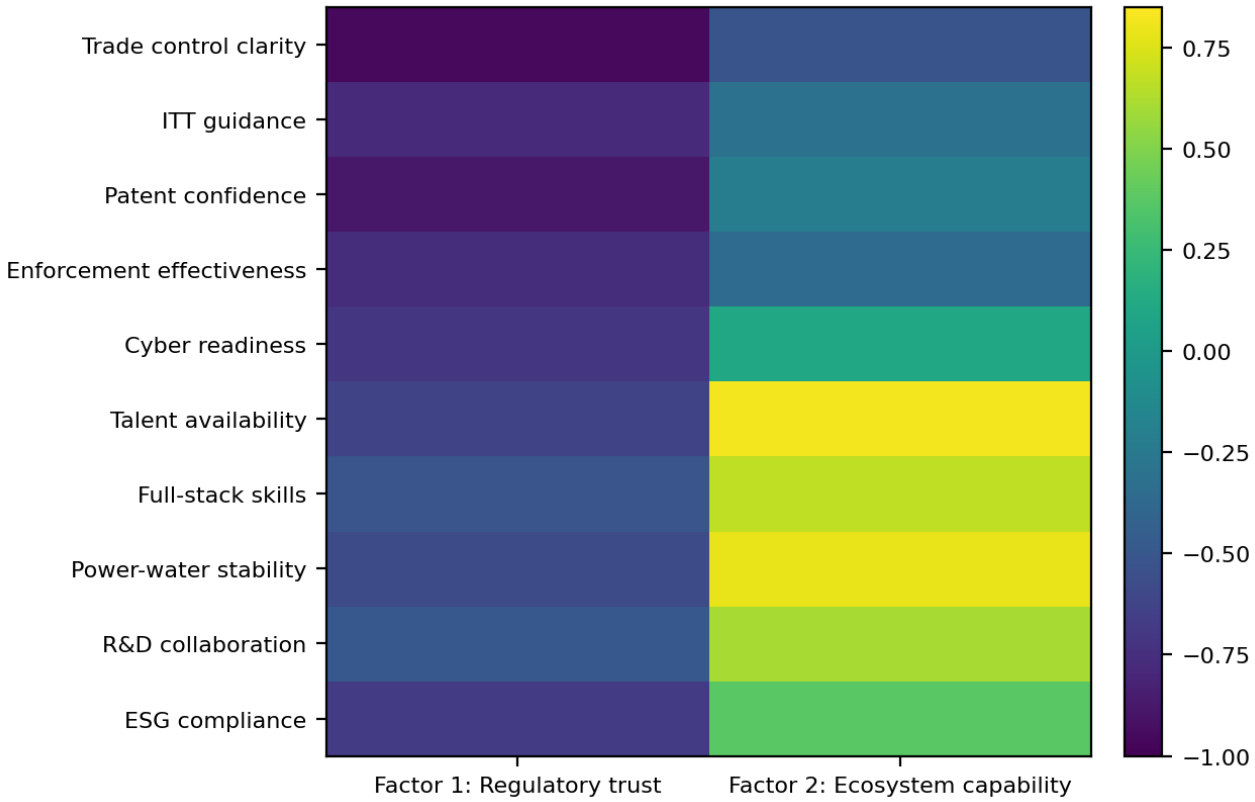


Figure 2. Illustrative synthetic factor loadings separating regulatory trust from ecosystem capability

Methodological note: the visualization uses synthetic data to demonstrate how future stakeholder surveys could be analyzed; it is not presented as actual fieldwork evidence in this paper.

Cyber-physical security reinforces these concerns. Semiconductor customers need assurance that production lines, cleanroom access, data environments, and supplier interactions are protected against compromise. The challenge is especially acute for ATP facilities handling multiple customers or proprietary process flows. Vietnam's industrial parks and high-tech zones will increasingly need standardized expectations for secure facility operations, incident reporting, vendor qualification, and trusted data environments. Without those expectations, it will be difficult to institutionalize a credible trusted-ATP proposition.

Figure 2 provides an illustrative synthetic two-factor view of how future stakeholder-survey data could separate perceptions of regulatory trust from perceptions of ecosystem capability. Although the data are synthetic and intended only as a methodological demonstration, the figure is useful because it shows why policy reform and industrial upgrading should be analyzed together rather than in isolation.

These findings suggest that Vietnam should avoid treating trust solely as a diplomatic label or branding exercise. A country becomes trusted when investors can see the legal basis, the procedures, the trained people, and the track record that make sensitive collaboration less risky. Vietnam has begun building that architecture. The next phase is to make it routine.

D. US Partnership Instruments and Trust-Building

Vietnam's trust-building agenda aligns closely with the United States' broader effort to diversify and secure semiconductor supply chains among partners. The 2023 US-Vietnam Comprehensive Strategic Partnership explicitly included a new semiconductor partnership and US support for workforce and ecosystem development. This political commitment matters because it signals that semiconductor cooperation is embedded in a higher-level strategic relationship rather than in isolated firm-to-firm deals.

The most relevant operational instrument is the International Technology Security and Innovation Fund. Congressional Research Service analysis explains that the ITSI Fund provides $500 million over five years for the Department of State to work with foreign partners on secure and trusted

telecommunications and semiconductor supply-chain activities. CSIS has argued that the fund's importance lies not simply in its budget size, but in its ability to catalyze standards-setting, workforce development, secure ecosystem planning, and partner-country capacity building. This is particularly relevant for Vietnam, which does not need only more capital; it needs institutional acceleration.

The partnership agenda is already taking practical form. In 2024, the US Department of State awarded Arizona State University $13.8 million under an ITSI-related initiative to support assembly, testing, and packaging capabilities in partner countries, including workforce development in the Indo-Pacific. The US-Vietnam CSP also referenced initial seed funding for semiconductor workforce initiatives. These efforts are useful because they target areas where trust and capability reinforce each other: curricula, labs, secure training environments, and ecosystems of practice.

For Vietnam, the most productive US-linked partnership mechanisms fall into four baskets. The first is workforce and training: joint curricula, train-the-trainer programs, faculty mobility, shared labs, and industry placements. The second is compliance capacity-building: support for export-control offices, ICP implementation, customs and licensing modernization, and research-security practices. The third is R&D and prototyping cooperation: trusted access to design tools, shared testbeds, multi-project wafer pathways, and secure collaboration procedures. The fourth is ecosystem assurance: the development of auditable trusted-ATP or trusted-packaging standards, cyber-physical assessments, and traceability practices that help Vietnamese sites qualify for more sensitive work.

The broader result is that US partnership should not be framed narrowly as a source of funding or external endorsement. Its strategic value lies in helping Vietnam build the institutions through which trust becomes durable, auditable, and internationally legible.

VII. Discussion

Vietnam's semiconductor roadmap is increasingly ambitious and concrete. The policy architecture now includes an industry strategy, a dedicated human-resources program, and a strategic trade control decree. Major multinational and domestic projects are underway. US-Vietnam ties provide geopolitical and institutional support. Yet the central argument of this paper is that capacity expansion alone will not produce trusted ecosystem status. Trust must be co-produced by ministries, customs authorities, industrial parks, universities, domestic firms, foreign-invested enterprises, and partner-country institutions. It is therefore a governance challenge as much as an industrial one.

Three strategic implementation risks stand out.

The **first** is a timing mismatch between industrial expansion and institutional capacity. Investment can move faster than governance. Vietnam may continue to attract ATP and related projects even while its compliance, ITT, and IP systems lag behind. That would be preferable to stagnation, but it creates two dangers. One is that Vietnam becomes associated primarily with lower-trust segments while higher-value work remains elsewhere. The second is that a governance failure in a high-visibility case - such as an IP dispute, a sensitive export-control incident, or a major security lapse - could shape perceptions more powerfully than a large number of successful routine operations. This is why institutional readiness must be developed in parallel with investment attraction rather than after the fact.

A critical implementation hurdle in addressing this timing mismatch is inter-agency coordination. Operating a trusted ecosystem does not depend on a single ministry but requires synchronization across multiple state organs. For example, Decree No. 259/2025/ND-CP will only be credible if there are practical inter-agency licensing workflows and if customs authorities and sectoral regulators possess the technical expertise to differentiate ordinary trade from strategic trade. Therefore, developing ministry-level guidance and training specialized reviewers are decisive steps to translate legal texts into an actual, coordinated compliance culture. The **second** risk is the possibility of an assembly trap. Vietnam's success in ATP and electronics manufacturing is real, and it should not be dismissed. But if domestic firms, universities, and research institutions do not progressively gain capability in design, validation, software-tool usage, secure testing, supplier services, and applied R&D, the ecosystem may remain shallow. Foreign-invested facilities can create jobs and exports without generating sufficient domestic control over higher-value knowledge assets. The risk is not unique to Vietnam. Pacific Forum's India Technology Policy

papers repeatedly show how ecosystem development can stall when policy focuses too heavily on one visible segment while underinvesting in innovation, design capability, and institutional support for IP and R&D. The lesson for Vietnam is not to deprioritize ATP. It is to use ATP as the foundation for capability upgrading rather than as an endpoint.

The **third** risk concerns the balance between openness and security. Vietnam's growth model has long depended on openness to trade, FDI, and external partnerships. Semiconductor trust-building, however, requires more screening, more documentation, more internal controls, and in some cases more differentiated treatment of projects or knowledge flows. If these systems are poorly designed, they could create friction, delay, and uncertainty that weaken Vietnam's attractiveness. The solution is not to avoid controls, but to make them transparent, proportionate, and administratively competent. A clear, rules-based compliance system strengthens rather than weakens trust. In fact, the existence of a credible strategic trade control framework can make some partners more willing to deepen cooperation because it reduces ambiguity.

A related discussion concerns the role of domestic institutions. Trusted semiconductor ecosystems are rarely built through ministries alone. Universities need secure research governance. Industrial parks need security and continuity standards. Courts and enforcement bodies need technical familiarity. Domestic firms need compliance officers, contractual discipline, and IP strategy. This means ecosystem policy must be more distributed than conventional industrial policy. The state can set targets and provide incentives, but trust emerges only when many organizations internalize the relevant practices. This is why training and institution-building are so important. The challenge is not simply to produce more engineers, but to produce organizations that know how to handle sensitive technology responsibly.

Comparative insights reinforce this point. Taiwan's strength comes not only from fabs, but from the density of relationships among state research, universities, suppliers, and firms. South Korea's strength depends on industrial scale, but also on sustained institutional coherence. The United States remains central because its design, research, capital, and legal systems reinforce one another. Vietnam's route will necessarily differ, but the underlying pattern holds: trust is a systems property. It arises when many parts of the ecosystem are predictable and mutually supportive.

This broader perspective also clarifies the role of the United States. US-Vietnam semiconductor cooperation should not be understood only as an opportunity for Vietnam to receive capital or technical assistance. It is also an opportunity for Vietnam to align parts of its governance architecture with the expectations of a leading technology power and its allies. That alignment is not synonymous with dependency. On the contrary, institutional strengthening in compliance, research security, trade-secret protection, and trusted ATP can improve Vietnam's sovereignty by increasing its bargaining power and by enabling domestic firms to participate more deeply in high-value segments.

The policy implication is that Vietnam should think in terms of credible specialization. It does not need to dominate the full semiconductor stack. It needs to become trusted and competitive in carefully chosen segments, while building the institutions that permit gradual upgrading into adjacent higher-value functions. This approach is more realistic than immediate end-to-end self-sufficiency and more strategically valuable than pure assembly-led growth.

VIII. Institutional Reform and Partnership Roadmap

Vietnam now has enough policy momentum to move from general ambition to sequenced implementation. Table 3 summarizes the phased roadmap proposed in this section. The challenge is to prioritize reforms that simultaneously deepen trust, support industrial upgrading, and remain administratively feasible. The roadmap proposed here is therefore organized in phases and guided by the six-dimensional trust framework.

Table 3. Phased policy reform and partnership roadmap, 2026-2030

Phase	Policy reform priorities	US and allied partnership mechanisms	Expected outcome
2026-2027 Foundation	Implement Decree 259/2025; establish inter-agency licensing workflow; launch ICP pilots; publish ITT and research-security guidance; coordinate shared-lab and curriculum planning	ITSI-supported compliance training; joint curricula; train-the-trainer programs; pilot secure research environments	A credible baseline for trusted participation and a first cohort of compliance-ready institutions
2027-2028 Scaling	Strengthen IP and trade-secret enforcement; standardize cyber-physical security requirements for high-tech parks and critical suppliers; expand workforce pipelines and supplier-development programs	Regulator exchanges; trusted-lab cooperation; joint prototyping access; secure supply-chain standards and audits	Broader ecosystem depth, more reliable enforcement, and improved eligibility for higher-value ATP and design-adjacent work
2029-2030 Assurance and upgrading	Institutionalize trusted-ATP certification; implement traceability and anti-counterfeit measures; tie incentives more closely to R&D localization and validation capability	Mutual recognition pathways; public-private consortia; deeper collaboration in specialized chips, packaging, and secure test environments	Vietnam recognized as a trusted node for advanced back-end work and selected higher-value semiconductor functions

The first phase, covering roughly 2026-2027, should focus on foundation-building. The immediate priority is to operationalize Decree No. 259/2025/ND-CP rather than simply celebrate its adoption. Ministries should issue implementing guidance for semiconductor-relevant categories of dual-use goods, establish a practical inter-agency licensing workflow, and clarify the role of internal compliance programs for firms in the semiconductor ecosystem. Pilot ICP certification should be encouraged for early adopters among multinational firms, Vietnamese champions, and universities involved in advanced semiconductor work. This would create demonstrator cases and help build a domestic community of compliance practice.

During the same period, Vietnam should publish national guidance on intangible technology transfer and research security for universities, labs, and technology firms. The guidance should cover classification of sensitive technical information, foreign collaboration review, cloud and data access governance, contractual safeguards, and procedures for escalating potential controlled-technology concerns. The objective is not to securitize all research, but to establish clear institutional routines for work that intersects with sensitive semiconductor technology.

The first phase should also prioritize workforce system design. Decision No. 1017 provides quantitative targets, but delivery requires curriculum alignment, faculty training, and shared-use lab investment. Vietnam should therefore establish a national semiconductor education consortium linking key universities, the National Innovation Center, industry partners, and selected foreign institutions. This consortium should coordinate curriculum standards, faculty development, tool access, and internship pathways. It should also include training modules on compliance, IP, quality systems, and secure data handling so that workforce policy supports trusted ecosystem goals from the outset.

US partnership mechanisms can be most useful in this foundation phase by supporting training labs, compliance systems, and secure research environments. ITSI-related cooperation, university partnerships, and industry-linked programs should be directed not only to generic workforce expansion but to the creation of trusted institutional interfaces:

export-control offices, research-security practices, secure lab protocols, and applied curriculum on advanced packaging and design.

The second phase, roughly 2027-2028, should emphasize scaling and enforcement capability. By this point, Vietnam should move from guidance to institutionalization in three areas. First, IP and trade-secret protection should be strengthened through specialized dockets, designated technical adjudicators, or specialized units that can handle complex high-technology disputes more effectively. Second, cyber-physical security expectations should be standardized for high-tech parks and critical suppliers. This does not require a one-size-fits-all regime, but it does require minimum standards for facility security, incident response, data segregation, and supplier integrity. Third, ICP adoption and trade-control implementation should be extended beyond flagship firms to a wider group of ecosystem participants, including critical service providers and research organizations.

This phase should also focus on deeper industrial upgrading. Vietnam should create incentives linked not only to capital investment but to local capability formation: joint labs, validation work, engineering service centers, secure testing environments, and supplier-development programs. Domestic firms such as FPT and Viettel should be encouraged to move into areas that complement rather than duplicate multinational activity - for example, packaging-related software, validation, application-specific design, edge-AI hardware integration, and secure subsystem development. Carefully designed R&D-linked incentives can help reduce the risk that Vietnam's ecosystem remains dominated by foreign-owned back-end enclaves.

Partnership with the United States and other like-minded economies in this scaling phase should broaden from training to standards and implementation support. Useful mechanisms include regulator-to-regulator exchanges on export controls and IP enforcement, joint prototyping pathways, access to trusted lab environments, and collaborative work on supply-chain assurance practices. Industry associations can play an important role here because trusted ecosystem standards often emerge from repeated interaction among firms, regulators, and sector bodies rather than from government decree alone.

The third phase, roughly 2029-2030, should be centered on assurance and upgrading. By this stage, Vietnam should aim to institutionalize a trusted-ATP framework that allows qualified sites to demonstrate compliance, security, traceability, and operational reliability in a standardized way. Such a framework could combine self-assessment, third-party audit, and government recognition, with stricter tiers for sites handling more sensitive work. The value of this approach is signaling. It gives foreign customers and partner governments a more concrete basis for evaluating Vietnamese facilities and it creates incentives for sites to invest in governance capability rather than relying solely on cost advantages.

This phase should also tie incentives more closely to R&D localization and higher-value activities. For example, additional support could be linked to domestic design collaboration, packaging-related process development, secure testing IP, or joint workforce programs. The objective is not to force localization prematurely, but to reward firms that help thicken the ecosystem. Mutual-recognition pathways with partner countries or industry associations could also be explored, especially where Vietnam seeks to qualify as a trusted location for specific ATP or validation functions.

Across all phases, five cross-cutting policy principles should guide implementation.

First, trust reforms should be transparent and administratively simple wherever possible. Firms are more likely to support compliance systems when rules are clear, timelines are predictable, and responsibilities are not fragmented across too many agencies.

Second, workforce policy should be treated as an institutional policy, not just an educational one. Training targets must be matched with shared labs, tool access, faculty incentives, internships, and applied research channels.

Third, domestic capability should be nurtured through complementarity. Vietnam does not need to replace multinational investment; it needs to build local firms and institutions that can connect to it at higher levels of value creation.

Fourth, security and openness should be jointly optimized. Vietnam's advantage lies partly in being open, pragmatic, and partnership-oriented. Security

measures should therefore be designed to increase confidence, not to create unnecessary opacity or burden.

Fifth, partnership should be outcome-oriented. Cooperation with the United States and other partners should be evaluated by whether it leaves behind durable Vietnamese capability - trained people, functioning labs, stronger compliance systems, better enforcement practices, and more trusted sites.

In summary, the roadmap is not a call for maximalism. It is a call for sequenced institution-building. Vietnam already has momentum in investment and strategy. The next step is to ensure that the ecosystem can be trusted with progressively more valuable and more sensitive semiconductor work.

IX. Conclusion and Future Work

Vietnam is entering a decisive phase in its semiconductor trajectory. The country now combines strong back-end momentum, a national development strategy, an ambitious workforce agenda, growing international partnerships, and a newly established strategic trade control framework. These developments show that Vietnam is no longer merely an observer of semiconductor restructuring; it is an emerging participant with real policy and industrial weight.

The central argument of this paper is that industrial momentum alone will not determine whether Vietnam secures a durable place in trusted semiconductor supply chains. The decisive variable is institutional trust. Firms and partner governments will deepen engagement where they believe that sensitive technology can be protected, compliance obligations can be met, IP can be enforced, cyber-physical risks can be managed, and skilled personnel can operate within predictable and secure organizations. In this sense, the next stage of Vietnam's semiconductor development is fundamentally a governance project.

Vietnam has already taken important steps. Decision No. 1017 and Decision No. 1018 provide strategic direction on human capital and industrial ambition. Decree No. 259/2025/ND-CP begins to create the compliance architecture needed for participation in a more security-conscious technology order. US-Vietnam cooperation under the Comprehensive Strategic Partnership and related ITSI-linked efforts offers a pathway to accelerate not only capacity but also institutional credibility. The country therefore has an unusual opportunity: it can build trust institutions at an early stage rather than retrofitting them after the ecosystem is already large and fragmented.

The policy recommendation is straightforward: Vietnam should pursue credible specialization rather than symbolic comprehensiveness. It should deepen leadership in ATP and adjacent services while building the institutional systems that enable expansion into design support, validation, secure R&D, and selected higher-value functions. This requires an integrated policy stack: strategic trade control implementation, ITT governance, stronger IP and trade-secret enforcement, secure industrial and research environments, and a workforce system tied directly to ecosystem needs. Such an approach is more realistic than immediate pursuit of full-spectrum semiconductor self-sufficiency and more valuable than a narrow assembly-led path.

Future research should focus on three priorities. First, fieldwork should test how multinational firms, domestic firms, universities, regulators, and partner-country officials rank the relative importance of trade controls, ITT governance, IP protection, cybersecurity, infrastructure, and talent in location decisions. Second, firm-level case studies are needed to understand how compliance and security practices actually operate inside ATP and design-adjacent facilities in Vietnam. Third, future policy work should develop measurable ecosystem-assurance indicators that allow Vietnam to monitor progress from capacity building to trusted participation.

Vietnam's semiconductor opportunity is real, but it will be won or lost in the details of institution-building. The countries that matter most in the next phase of semiconductor globalization will not necessarily be those that promise everything. They will be those that can reliably deliver specific functions within trusted networks. Vietnam is well positioned to become one of them if it treats trust not as a slogan, but as a national capability.

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